1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
02		248015	ENGINEERING RELEASED	12/05/02	?

SCHEM,MLB,PB15

Fri Jan 23 20:30:40 2004

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7447 MAXBUS INTERFACE
6	MPC7447 DATA / NC PINS / BOOTBANGER
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	400PIN STACKED DDR SODIMM CONNECTOR
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS/1.5V LDO
16	INTREPID DECOUPLING
17	USB 2.0 INTERFACE (uPD720101)
18	CARDBUS INTERFACE (PCI1510)
19	M10 AGP INTERFACE & SPREAD SPECTRUM SUPPORT External TMDS (DVI Transmitter SIL1162)
20	M10 LVDS/TMDS/GPIO & GPU VCORE
21	M10 POWER

PAGE	CONTENTS
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO, LVDS
23	KBD,TPAD,HALL EFFECT,PWR BUTTON,LMU/SENSOR
24	INTERNAL CONNECTORS - AIRPORT, HARD DRIVE, OPTICAL DRIVE
25	FAN CONTROLLER, USB MODEM/SOFT MODEM, SOUND/LEFT USB/BLUETOOTH, SERIAL DEBUG
26	GIGABIT ETHERNET INTERFACE
27	FIREWIRE PHY
28	FIREWIRE PORTS
29	PMU
30	BATTERY CHARGER AND CONNECTOR
31	PBUS SUPPLY / PMU SUPPLY / BACKUP BATTERY
32	3.3V / 5V SYSTEM POWER SUPPLY
33	CPU CORE VOLTAGE POWER SUPPLY
34	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
35	SIGNAL CONSTRAINTS (1 OF 4) - DDR MEM/CLK
36	SIGNAL CONSTRAINTS (2 OF 4) - CPU
37	SIGNAL CONSTRAINTS (3 OF 4) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (4 OF 4) - POWER NETS
39	FUNCTIONAL TESTPOINTS
40	REVISION HISTORY
41	SIGNAL LOCATIONS
42	COMPONENT LOCATIONS (1 OF 2)
43	COMPONENT LOCATIONS (2 OF 2)

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
SSCG	NO_SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
USB_MODEM	SOFT_MODEM
GPU_PWRMSR	INT_TMDS
GPU_SS	
VGA_BUFFER_RES	
EXT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6338	1	SCHEM,MLB,PB15	SCH1	
820-1441	1	PCBF,MLB,PB15	PCB1	
065-3951	1	CMNPRTS,MLB,PB15	DMS1	DMS630-4285&DMS630-4721
065-3952	1	SELPRTS,MLB,PB15,BTR	DMS2	DMS630-4285
065-4479	1	SELPRTS,MLB,PB15,BST	DMS3	DMS630-4721

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

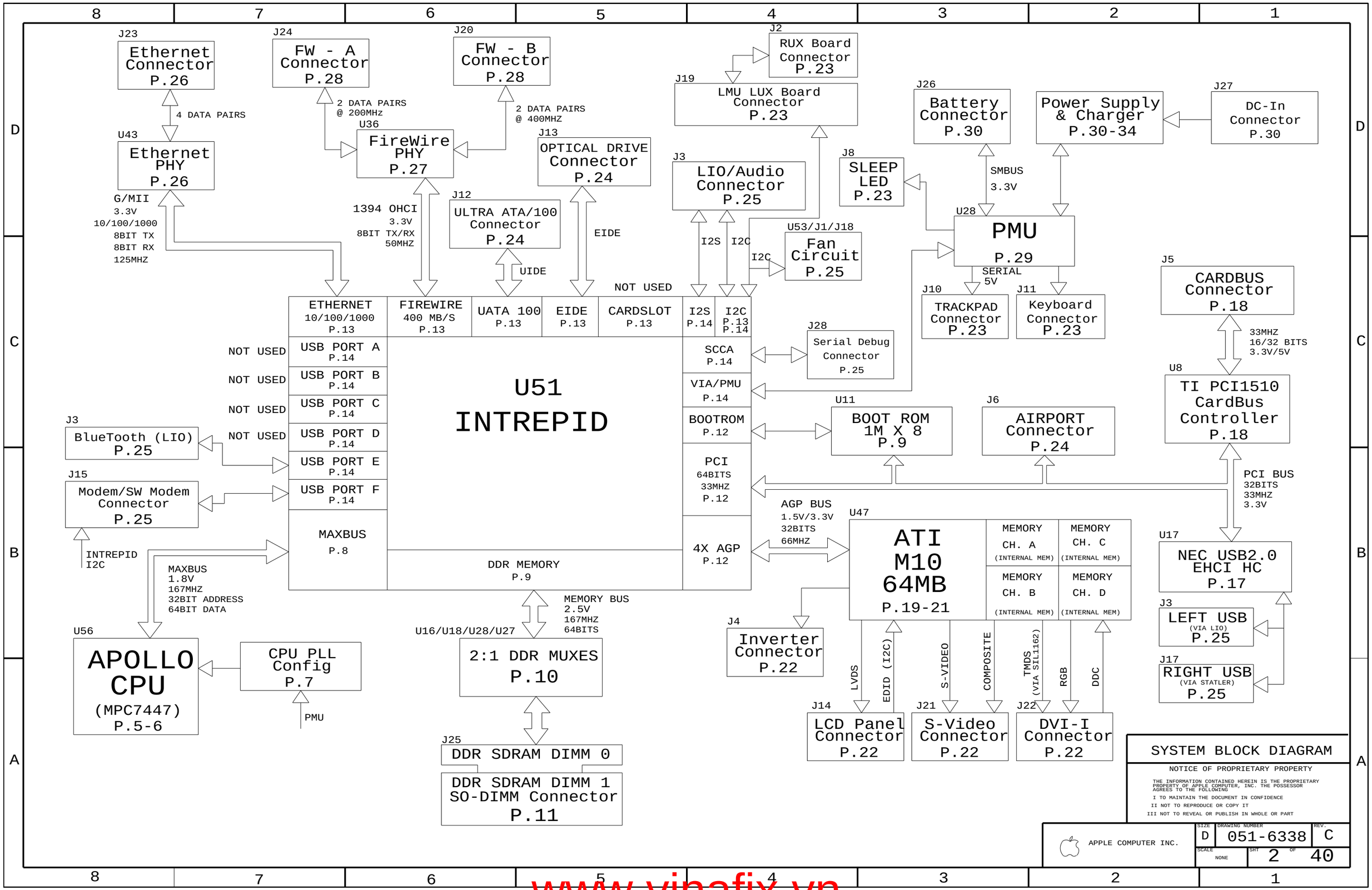
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TITLE
SCHEM,MLB,PB15"

DRAWING NUMBER 051-6338 REV. C

SHT 1 OF 40

www.vinafix.vn



www.vinafix.vn

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>-13.44V TURNS-ON
<-13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

14V_PBUS

+3V_PMU LDO PG 31

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
STBYMD
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

DC/DC (LTC3411) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

+1.8V_MAIN

MAXBUS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

DCDC_EN
SLEEP

GPU_VCORE SEQUENCING

D3_COLD

+5V_MAIN

VCC
EXT_VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

DCDC_EN
SLEEP

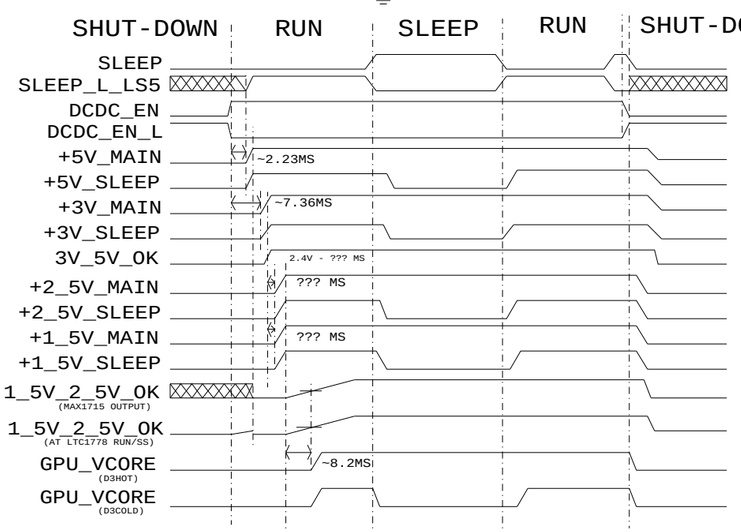
MAXBUS SEQUENCING

+PBUS

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)



POWER BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 3 OF 40	

www.vinafix.vn

PCB SPECS

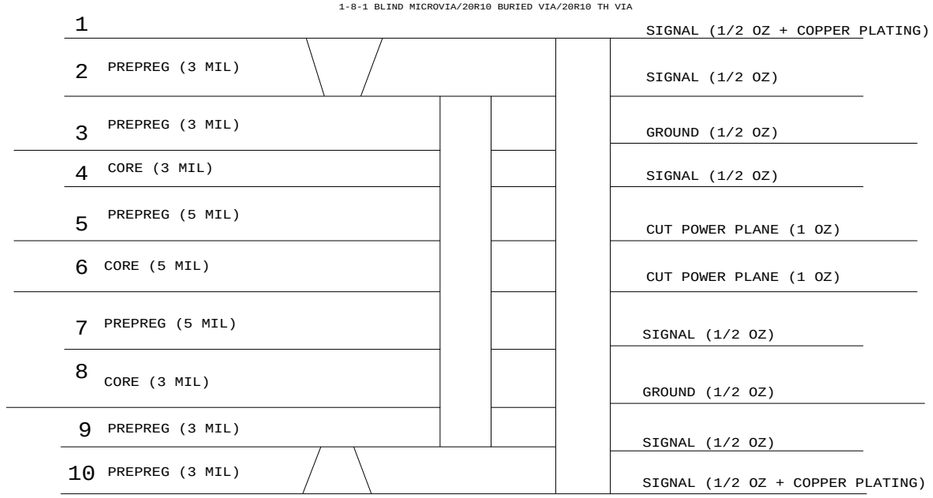
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10 LEFT CPU
ZT21 HOLE-VIA-20R10 UPPER RT GPU
ZT58 HOLE-VIA-20R10 LWR CPU
ZT59 HOLE-VIA-20R10 LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI — CHGND2
ZT86 HOLE-VIA-20R10 DVI 1394 — CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR — CHGND5

INVERTER

SH1 OG-503040 SHLD-SM — CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 — ZT301_SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 — ZT302_SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 — ZT10_SPN NO_TEST=TRUE

GROUND VIAS

ZT76, ZT28, ZT72, ZT69, ZT68, ZT64, ZT61, ZT38, ZT39, ZT40, ZT41, ZT46, ZT71, ZT78, ZT80 HOLE-VIA-20R10

ZT50, ZT51, ZT52, ZT53, ZT57, ZT60, ZT82, ZT22, ZT17, ZT35, ZT45, ZT79, ZT81, ZT83, ZT49 HOLE-VIA-20R10

ZT48, ZT47, ZT54, ZT55, ZT56, ZT84, ZT5, ZT15, ZT44, ZT4, ZT8, ZT6, ZT32, ZT3, ZT10 HOLE-VIA-20R10

ZT11, ZT34, ZT20, ZT43, ZT70, ZT2, ZT9, ZT75, ZT73, ZT63, ZT77, ZT66, ZT62, ZT65, ZT13 HOLE-VIA-20R10

ZT25, ZT19, ZT24, ZT67, ZT37, ZT29, ZT31, ZT1, ZT14, ZT12, ZT27, ZT26, ZT30, ZT33, ZT18 HOLE-VIA-20R10

BOARD INFORMATION

NOTICE OF PROPRIETARY PROPERTY

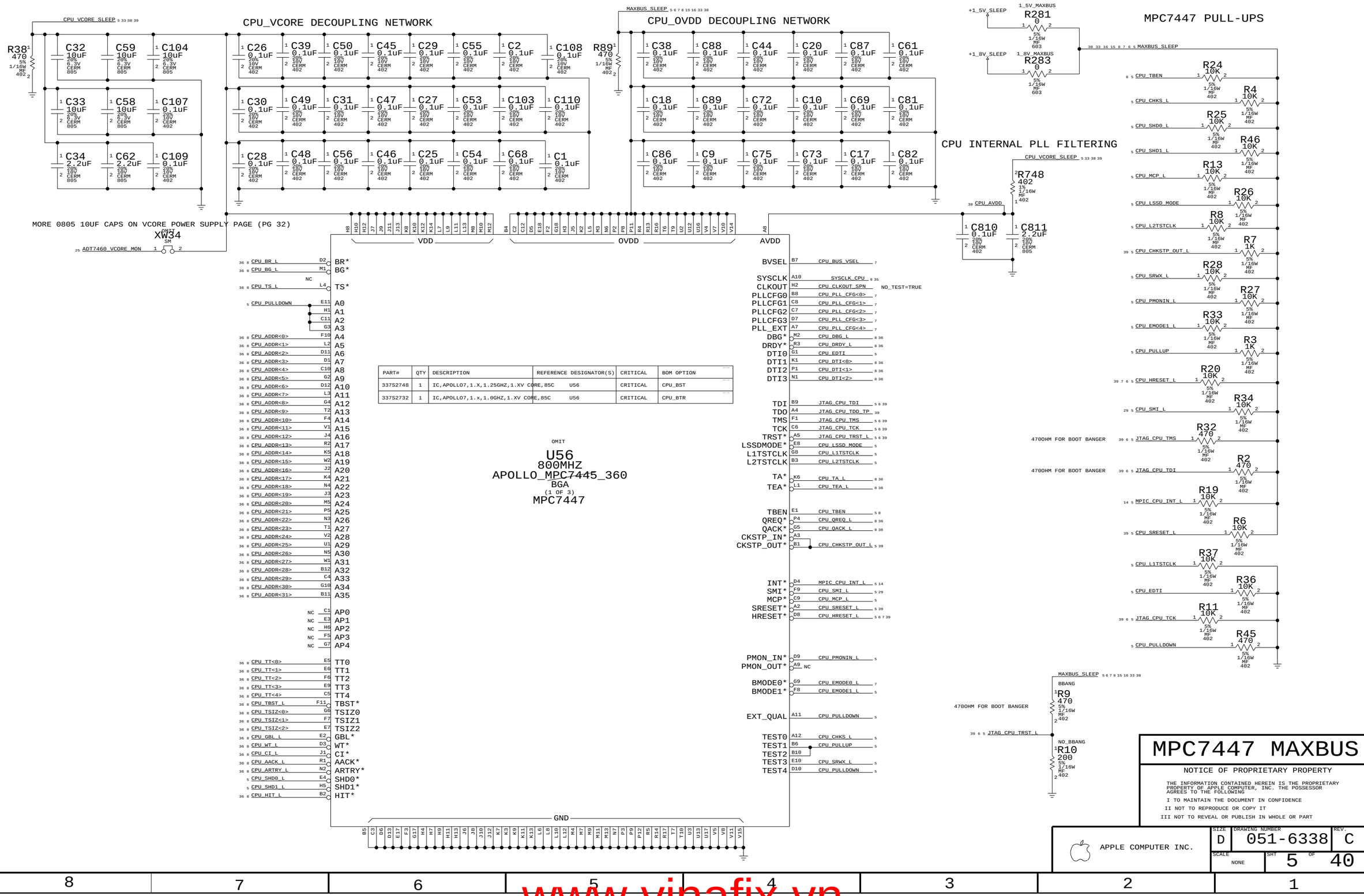
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 4 OF 40	

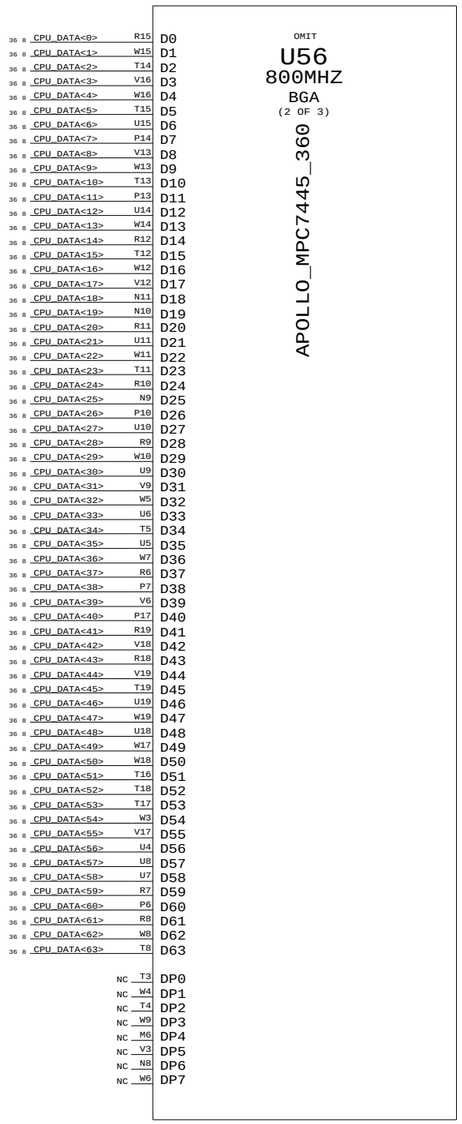
www.vinafix.vn

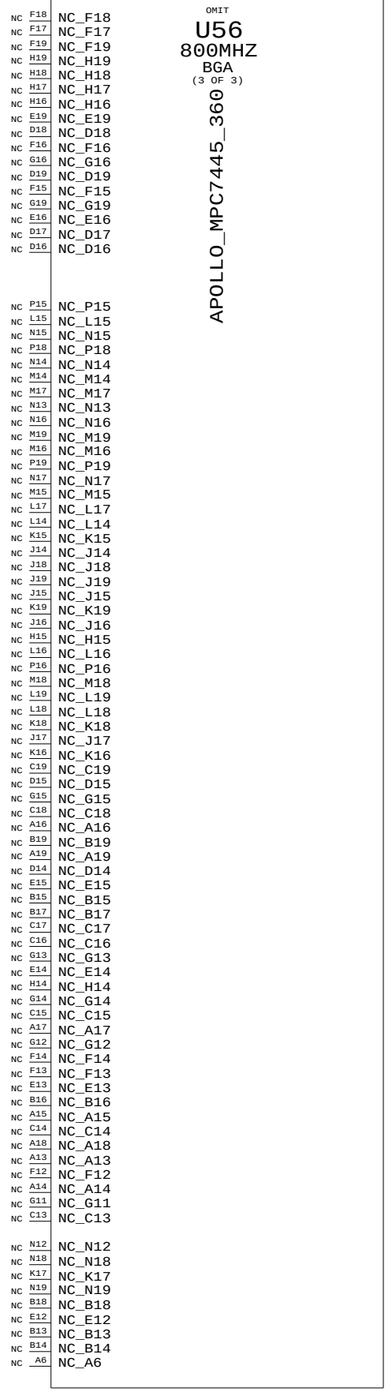


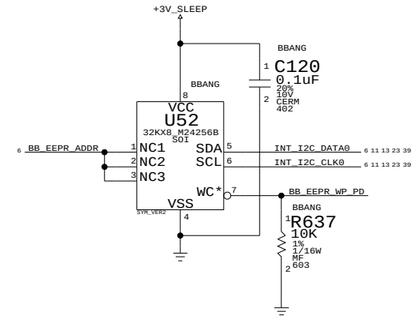
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2748	1	IC,APOLLO7,1.X,1.25GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BST
337S2732	1	IC,APOLLO7,1.X,1.0GHZ,1.XV CORE,85C	U56	CRITICAL	CPU_BTR

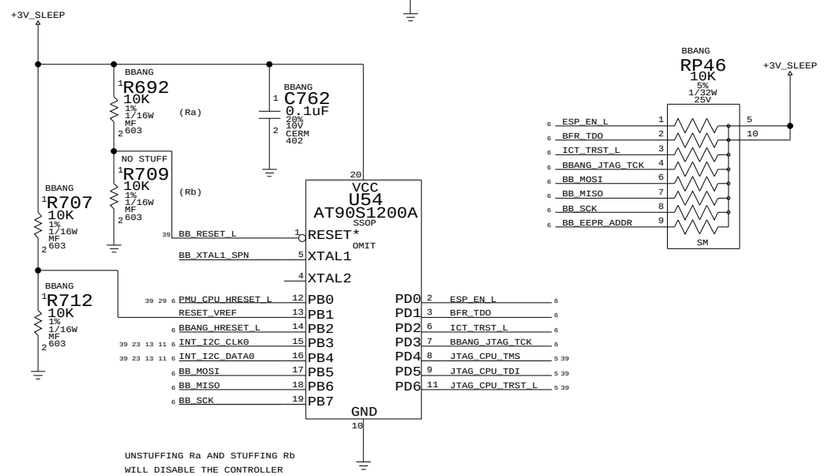
www.vinafix.vn

BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON



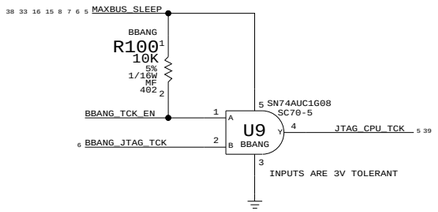


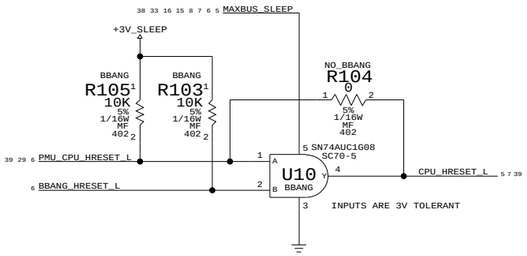




UNSTUFFING Ra AND STUFFING Rb
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	000-8248-FW-ST4 BBANGER MCU,PROGRAMMED W/ BBANGER	U54	BBANG





MPC7447/BBANG

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

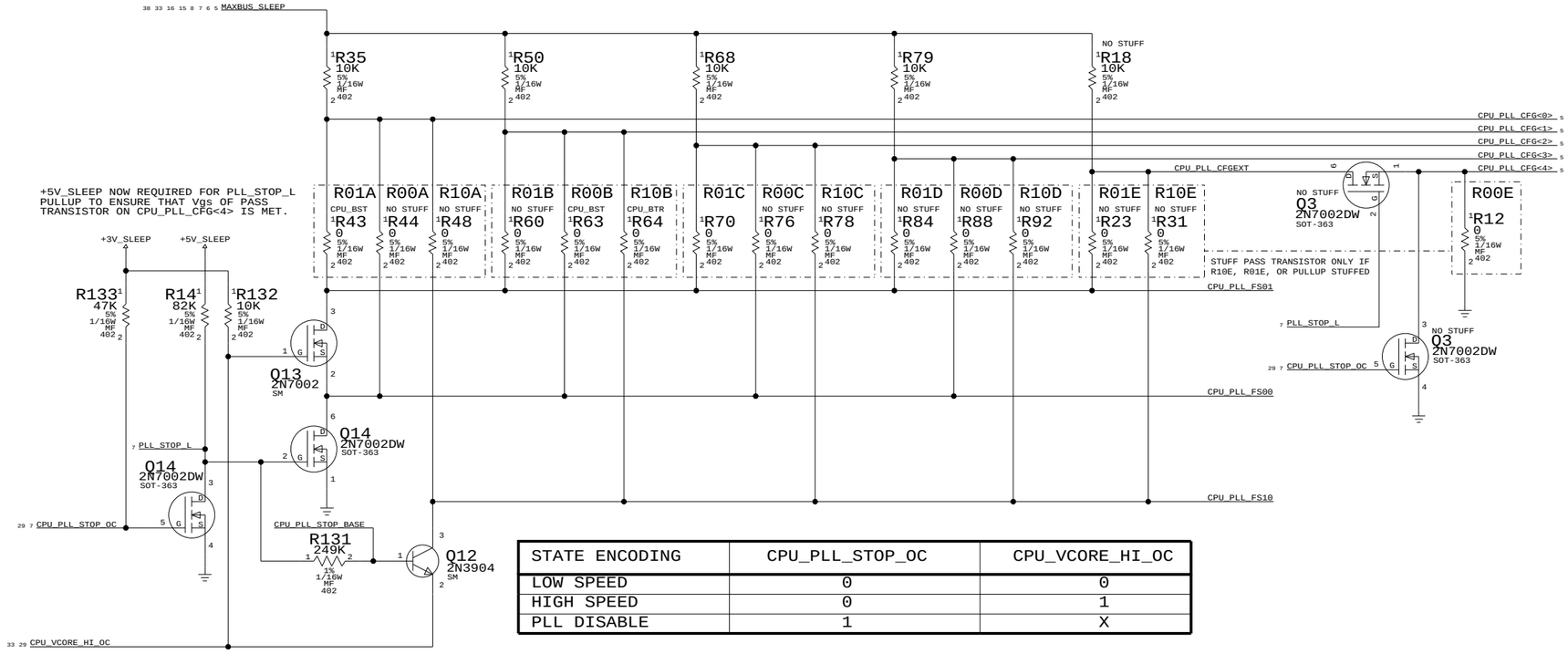
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 6 OF 40	

www.vinafix.vn

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

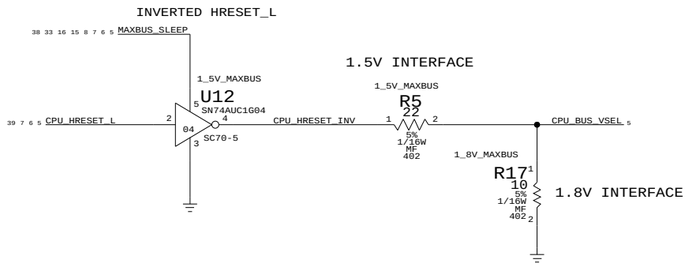
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

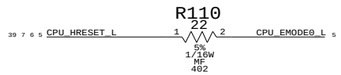
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

CPU CONFIGURATION

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV: C

SCALE NONE | SHT 7 OF 40

www.vinafix.vn

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

NO STUFF R640[1] 10K	NO STUFF R639[1] 10K	NO STUFF R638[1] 10K	NO STUFF R666[1] 10K	R622[1] 10K	R619[1] 10K	R618[1] 10K	R653[1] 10K
CPU_DATA<32>	CPU_DATA<33>	CPU_DATA<34>	CPU_DATA<35>	CPU_DATA<36>	CPU_DATA<37>	CPU_DATA<38>	CPU_DATA<39>
0: DDR_TRDYEN Pull down 1: TDI output (Age)	Analyzerclk_En_h 0: Active low 1: Active	DDR_TRDYEN Pull down 0: Active low 1: Active	Bypass_Sync_Pll 0: Active low 1: Active	Spare	Spare	Spare	Spare

BIT 40 TO 47

MAXBUS_SLEEP

NO STUFF R641[1] 10K	SSCG R665[1] 10K	NO STUFF R664[1] 10K	NO_SSCG R693[1] 10K	NO STUFF R694[1] 10K	NO STUFF R699[1] 10K	R648[1] 10K	R677[1] 10K
CPU_DATA<40>	CPU_DATA<41>	CPU_DATA<42>	CPU_DATA<43>	CPU_DATA<44>	CPU_DATA<45>	CPU_DATA<46>	CPU_DATA<47>
R623[1] 10K	NO_SSCG R651[1] 10K	R649[1] 10K	SSCG R678[1] 10K	R679[1] 10K	R684[1] 10K		
Spare	Spare	BIT2	BIT1	BIT0	0: Internal Spread 1: Active	0: PLL5 (no spread) 1: PLL5 (no spread)	0: PLL4 (no spread) 1: PLL4 (no spread)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

SSCG R696[1] 10K	SSCG R695[1] 10K	NO STUFF R667[1] 10K	NO STUFF R668[1] 10K	NO STUFF R643[1] 10K	NO STUFF R642[1] 10K	NO STUFF R698[1] 10K	CPU_DATA<48>
CPU_DATA<49>	CPU_DATA<50>	CPU_DATA<51>	CPU_DATA<52>	CPU_DATA<53>	CPU_DATA<54>	CPU_DATA<55>	
NO_SSCG R681[1] 10K	NO_SSCG R680[1] 10K	NO STUFF R654[1] 10K	R655[1] 10K	R625[1] 10K	R624[1] 10K	NO STUFF R683[1] 10K	R626[1] 10K
BUF_MREF_CLK_OUTEnable_h 0: MREF_CLK_OUT Active 1: Active	0: PLL5 1: External source	OBSOLETE (Should remain high) 0: BOOTROM on IDE/CardSlot 1: BOOTROM on PCI1	0: Disable TI 1394b workaround 1: Enable TI 1394b workaround TI PHY workaround	BIT2	BIT1	BIT0	Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7
C187 0.22uF 20% 6.3V CERM 402

U51 INTREPID-REV2.1 BGA (1 OF 9) CRITCAL

VDD15A_7 (PLL6) H26

CPU_BR_L	E29	BR INPUT
CPU_BG_L	E26	BG NO BUS KEEPER
CPU_TS_L	B27	TS NO BUS KEEPER
CPU_ADDR<0>	D24	A_0
CPU_ADDR<1>	D25	A_1
CPU_ADDR<2>	A27	A_2
CPU_ADDR<3>	E24	A_3
CPU_ADDR<4>	G23	A_4
CPU_ADDR<5>	B26	A_5
CPU_ADDR<6>	A26	A_6
CPU_ADDR<7>	D23	A_7
CPU_ADDR<8>	A25	A_8
CPU_ADDR<9>	E23	A_9
CPU_ADDR<10>	J22	A_10
CPU_ADDR<11>	B25	A_11
CPU_ADDR<12>	H22	A_12
CPU_ADDR<13>	G22	A_13
CPU_ADDR<14>	D22	A_14
CPU_ADDR<15>	B24	A_15
CPU_ADDR<16>	B23	A_16
CPU_ADDR<17>	E22	A_17
CPU_ADDR<18>	J21	A_18
CPU_ADDR<19>	G21	A_19
CPU_ADDR<20>	E21	A_20
CPU_ADDR<21>	A24	A_21
CPU_ADDR<22>	D21	A_22
CPU_ADDR<23>	A23	A_23
CPU_ADDR<24>	H20	A_24
CPU_ADDR<25>	B22	A_25
CPU_ADDR<26>	H21	A_26
CPU_ADDR<27>	A22	A_27
CPU_ADDR<28>	E20	A_28
CPU_ADDR<29>	B21	A_29
CPU_ADDR<30>	D20	A_30
CPU_ADDR<31>	A21	A_31
CPU_CI_L	G26	CI
CPU_GBL_L	A29	GBL
CPU_TBST_L	A28	TBST
CPU_TSIZ<0>	G24	TSIZ_0
CPU_TSIZ<1>	H24	TSIZ_1
CPU_TSIZ<2>	D26	TSIZ_2
CPU_TT<0>	E25	TT_0
CPU_TT<1>	G25	TT_1
CPU_TT<2>	B28	TT_2
CPU_TT<3>	D27	TT_3
CPU_TT<4>	J25	TT_4
CPU_WT_L	D28	WT
CPU_AACK_L	B29	AACK NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT INPUT - PU
CPU_QREQ_L	A32	QREQ INPUT - PD
CPU_QACK_L	G27	QACK NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ
INT_SUSPEND_ACK_L	AM8	SUSPENDACK

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

CPU_FB_IN
CPU_FB_OUT — NO BUS KEEPER - PU
ANALYZER_CLK — INPUT - PU
STOPCPUCLK — NO BUS KEEPER - ?
ACS_REF — NO BUS KEEPER - ?
CPU_CLK — NO BUS KEEPER - PU / NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

TBEN — NO BUS KEEPER - PU

VSSA_7 (PLL6) H25

MAXBUS INTERFACE

D_0	D10	CPU_DATA<0>
D_1	G12	CPU_DATA<1>
D_2	E11	CPU_DATA<2>
D_3	H11	CPU_DATA<3>
D_4	B9	CPU_DATA<4>
D_5	B8	CPU_DATA<5>
D_6	A9	CPU_DATA<6>
D_7	A8	CPU_DATA<7>
D_8	E12	CPU_DATA<8>
D_9	D11	CPU_DATA<9>
D_10	B10	CPU_DATA<10>
D_11	J13	CPU_DATA<11>
D_12	A10	CPU_DATA<12>
D_13	D12	CPU_DATA<13>
D_14	E13	CPU_DATA<14>
D_15	G13	CPU_DATA<15>
D_16	B11	CPU_DATA<16>
D_17	D13	CPU_DATA<17>
D_18	A11	CPU_DATA<18>
D_19	G14	CPU_DATA<19>
D_20	H14	CPU_DATA<20>
D_21	E14	CPU_DATA<21>
D_22	B12	CPU_DATA<22>
D_23	G15	CPU_DATA<23>
D_24	B13	CPU_DATA<24>
D_25	H15	CPU_DATA<25>
D_26	D14	CPU_DATA<26>
D_27	B14	CPU_DATA<27>
D_28	A12	CPU_DATA<28>
D_29	G16	CPU_DATA<29>
D_30	E15	CPU_DATA<30>
D_31	J16	CPU_DATA<31>
D_32	D15	CPU_DATA<32>
D_33	A14	CPU_DATA<33>
D_34	A13	CPU_DATA<34>
D_35	D16	CPU_DATA<35>
D_36	E16	CPU_DATA<36>
D_37	G17	CPU_DATA<37>
D_38	B15	CPU_DATA<38>
D_39	H17	CPU_DATA<39>
D_40	A15	CPU_DATA<40>
D_41	B16	CPU_DATA<41>
D_42	E17	CPU_DATA<42>
D_43	A16	CPU_DATA<43>
D_44	J18	CPU_DATA<44>
D_45	H18	CPU_DATA<45>
D_46	D17	CPU_DATA<46>
D_47	G18	CPU_DATA<47>
D_48	A17	CPU_DATA<48>
D_49	B17	CPU_DATA<49>
D_50	E18	CPU_DATA<50>
D_51	B18	CPU_DATA<51>
D_52	D18	CPU_DATA<52>
D_53	A18	CPU_DATA<53>
D_54	A19	CPU_DATA<54>
D_55	H19	CPU_DATA<55>
D_56	B19	CPU_DATA<56>
D_57	J19	CPU_DATA<57>
D_58	A20	CPU_DATA<58>
D_59	D19	CPU_DATA<59>
D_60	E19	CPU_DATA<60>
D_61	G19	CPU_DATA<61>
D_62	B20	CPU_DATA<62>
D_63	G20	CPU_DATA<63>
DBG	A30	CPU_DBG_L
DRDY	G28	CPU_DRDY_L
DTI_0	K25	CPU_DTI<0>
DTI_1	D29	CPU_DTI<1>
DTI_2	B30	CPU_DTI<2>
TA	E27	CPU_TA_L
TEA	E28	CPU_TEA_L

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402
R168 0 5% 1/16W MF 402
R161 1K 1% 1/16W MF 402

SYSCLK_LA_TP
INTREPID_ACS_REF
SYSCLK_CPU → SYSCLK_CPU_UF

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

INT_CPUFB_OUT	R155 0 5% 1/16W MF 402	INT_CPUFB_OUT_SHORT	R140 0 5% 1/16W MF 402
INT_CPUFB_OUT_NORM	NO STUFF R128 0 5% 1/16W MF 402	INT_CPUFB_LONG	
INT_CPUFB_IN	NO STUFF R146[1] 0 5% 1/16W MF 402	R147 0 5% 1/16W MF 402	INT_CPUFB_IN_NORM
	NO STUFF R141[1] 0 5% 1/16W MF 402	NO STUFF R136 0 5% 1/16W MF 402	

MAXBUS PULL-UPS

MAXBUS_SLEEP

RP3 10K	CPU_TS_L	RP3 10K	CPU_TA_L	RP3 10K	CPU_ARTRY_L	RP2 10K	CPU_BR_L
R152 10K	CPU_HIT_L	RP2 10K	CPU_DRDY_L	RP2 10K	CPU_TEA_L	RP2 10K	CPU_AACK_L
R150 10K	CPU_DBG_L	RP3 10K	CPU_BG_L	R151 10K	CPU_QREQ_L		

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

NO STUFF R669[1] 10K	NO STUFF R645[1] 10K	NO STUFF R697[1] 10K	NO STUFF R670[1] 10K	NO STUFF R644[1] 10K	NO STUFF R646[1] 10K	CPU_DATA<56>	CPU_DATA<57>
CPU_DATA<58>	CPU_DATA<59>	CPU_DATA<60>	CPU_DATA<61>	CPU_DATA<62>	CPU_DATA<63>		
R656[1] 10K	R685[1] 10K	R657[1] 10K	R628[1] 10K	R682[1] 10K	R658[1] 10K	NO STUFF R627[1] 10K	R629[1] 10K
Spare	Spare	OBSOLETE (Should remain high) ROM Overlay PCI1 0: 1-1 IDE / 2-3 PCI1 1: 0-1 IDE / 2-3 PCI1	PCI1_REQ2_L / PCI1_GNT2_L 0: REQ/GNT 1: GPIOs	PCI1_REQ1_L / PCI1_GNT1_L 0: REQ/GNT 1: GPIOs	PCI1_REQ0_L / PCI1_GNT0_L 0: REQ/GNT 1: GPIOs	Firewire PHY interface 0: A-Mode interface 1: B-Mode interface	Processor Bus Mode 0: 64x Bus (G4) 1: 72x Bus (G5)

Intrepid MaxBus

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 8 OF 40	

www.vinafix.vn

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U51
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	H35	DDR_A_0
DDR_DATA_1	AK33	G35	DDR_A_1
DDR_DATA_2	AK31	G36	DDR_A_2
DDR_DATA_3	AK35	F36	DDR_A_3
DDR_DATA_4	AK36	F35	DDR_A_4
DDR_DATA_5	AJ32	E35	DDR_A_5
DDR_DATA_6	AJ35	E36	DDR_A_6
DDR_DATA_7	AJ36	G32	DDR_A_7
DDR_DATA_8	AG33	D36	DDR_A_8
DDR_DATA_9	AG35	H36	DDR_A_9
DDR_DATA_10	AH35	G33	DDR_A_10
DDR_DATA_11	AG36	H33	DDR_A_11
DDR_DATA_12	AH36	D35	DDR_A_12
DDR_DATA_13	AH32	L30	DDR_BA_0
DDR_DATA_14	AG32	M29	DDR_BA_1
DDR_DATA_15	AG31	AN34	DDRCS_0
DDR_DATA_16	AE32	AN36	DDRCS_1
DDR_DATA_17	AF35	AL35	DDRCS_2
DDR_DATA_18	AF36	AL33	DDRCS_3
DDR_DATA_19	AE36	AJ31	DDR_DQS_0
DDR_DATA_20	AE35	AH31	DDR_DQS_1
DDR_DATA_21	AE33	AD32	DDR_DQS_2
DDR_DATA_22	AD36	AB30	DDR_DQS_3
DDR_DATA_23	AD35	V30	DDR_DQS_4
DDR_DATA_24	AA36	P32	DDR_DQS_5
DDR_DATA_25	AA35	N29	DDR_DQS_6
DDR_DATA_26	AA33	L32	DDR_DQS_7
DDR_DATA_27	AB36	AJ33	DDR_DM_0
DDR_DATA_28	AB35	AH33	DDR_DM_1
DDR_DATA_29	AC36	AD33	DDR_DM_2
DDR_DATA_30	AA32	AC35	DDR_DM_3
DDR_DATA_31	AB33	T35	DDR_DM_4
DDR_DATA_32	V36	T33	DDR_DM_5
DDR_DATA_33	U33	N32	DDR_DM_6
DDR_DATA_34	U32	L33	DDR_DM_7
DDR_DATA_35	V35	L29	DDRRAS
DDR_DATA_36	T36	H32	DDRCAS
DDR_DATA_37	U36	K30	DDRWE
DDR_DATA_38	U35	AN35	DDRCKE0
DDR_DATA_39	T34	AM35	DDRCKE1
DDR_DATA_40	P33	AM36	DDRCKE2
DDR_DATA_41	R36	AL36	DDRCKE3
DDR_DATA_42	P35	AB32	DDR_SELHI_0
DDR_DATA_43	P34	AE29	DDR_SELHI_1
DDR_DATA_44	R34	N30	DDR_SELLO_0
DDR_DATA_45	R35	T32	DDR_SELLO_1
DDR_DATA_46	R33	Y32	DDR_MCLK_0_P
DDR_DATA_47	R32	Y33	DDR_MCLK_0_N
DDR_DATA_48	N35	Y35	DDR_MCLK_1_P
DDR_DATA_49	M36	Y36	DDR_MCLK_1_N
DDR_DATA_50	L35	Y30	DDR_MCLK_2_P
DDR_DATA_51	M35	W30	DDR_MCLK_2_N
DDR_DATA_52	M33	W32	DDR_MCLK_3_P
DDR_DATA_53	L36	W33	DDR_MCLK_3_N
DDR_DATA_54	N33	V33	DDR_MCLK_4_P
DDR_DATA_55	M34	V32	DDR_MCLK_4_N
DDR_DATA_56	J32	W35	DDR_MCLK_5_P
DDR_DATA_57	J33	W36	DDR_MCLK_5_N
DDR_DATA_58	J35	AA22	DDR_REF
DDR_DATA_59	K32	Y22	DDR_VREF_0
DDR_DATA_60	K33	T22	DDR_VREF_1
DDR_DATA_61	J36		
DDR_DATA_62	K36		
DDR_DATA_63	K35		

’0’ & ’1’ GO TO SLOT A
’2’ & ’3’ GO TO SLOT B

’0’ & ’1’ GO TO SLOT A
’2’ & ’3’ GO TO SLOT B

’0’S ARE SAME POLARITY (ACTIVE-LO)
’1’S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

+2_5V_INTREPID
R208 10K 1% 1/16W MF 402
R202 10K 1% 1/16W MF 402
C249 0.1uF 20% 10V CERM 402
INT_MEM_VREF
R209 1K 1% 1/16W MF 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP20 22 4 5	SYSCLK_DDRCLK_A1	
SYSCLK_DDRCLK_A1_L_UF	RP20 22 3 6	SYSCLK_DDRCLK_A1_L	
SYSCLK_DDRCLK_A0_UF	RP22 22 1 8	SYSCLK_DDRCLK_A0	
SYSCLK_DDRCLK_A0_L_UF	RP22 22 2 7	SYSCLK_DDRCLK_A0_L	
SYSCLK_DDRCLK_B1_UF	RP20 22 2 7	SYSCLK_DDRCLK_B1	
SYSCLK_DDRCLK_B1_L_UF	RP20 22 1 8	SYSCLK_DDRCLK_B1_L	
SYSCLK_DDRCLK_B0_UF	RP22 22 3 6	SYSCLK_DDRCLK_B0	
SYSCLK_DDRCLK_B0_L_UF	RP22 22 4 5	SYSCLK_DDRCLK_B0_L	

CS

MEM_CS_L<0>	RP31 22 3 6	RAM_CS_L<0>
MEM_CS_L<1>	RP31 22 2 7	RAM_CS_L<1>
MEM_CS_L<2>	RP29 22 3 6	RAM_CS_L<2>
MEM_CS_L<3>	RP29 22 4 5	RAM_CS_L<3>

CKE

MEM_CKE<0>	RP31 22 1 8	RAM_CKE<0>
MEM_CKE<1>	RP31 22 4 5	RAM_CKE<1>
MEM_CKE<2>	RP29 22 1 8	RAM_CKE<2>
MEM_CKE<3>	RP29 22 2 7	RAM_CKE<3>

ADDR

MEM_ADDR<0>	RP14 22 3 6	RAM_ADDR<0>
MEM_ADDR<1>	RP12 22 2 7	RAM_ADDR<1>
MEM_ADDR<2>	RP12 22 1 8	RAM_ADDR<2>
MEM_ADDR<3>	RP12 22 4 5	RAM_ADDR<3>
MEM_ADDR<4>	RP12 22 3 6	RAM_ADDR<4>
MEM_ADDR<5>	RP9 22 2 7	RAM_ADDR<5>
MEM_ADDR<6>	RP9 22 1 8	RAM_ADDR<6>
MEM_ADDR<7>	RP14 22 2 7	RAM_ADDR<7>
MEM_ADDR<8>	RP9 22 4 5	RAM_ADDR<8>
MEM_ADDR<9>	RP14 22 4 5	RAM_ADDR<9>
MEM_ADDR<10>	RP14 22 1 8	RAM_ADDR<10>
MEM_ADDR<11>	RP17 22 4 5	RAM_ADDR<11>
MEM_ADDR<12>	RP9 22 3 6	RAM_ADDR<12>

BA

MEM_BA<0>	RP17 22 2 7	RAM_BA<0>
MEM_BA<1>	RP17 22 1 8	RAM_BA<1>

CNTL

MEM_WE_L	RP17 22 3 6	RAM_WE_L
MEM_CAS_L	R162 22 1 2	RAM_CAS_L
MEM_RAS_L	R176 22 1 2	RAM_RAS_L

1MB BOOT ROM

+3V_MAIN
C125 2.2uF 20% 10V CERM 805
C773 0.1uF 20% 10V CERM 402
C122 0.1uF 20% 10V CERM 402

U11
FEPR-1MX8
1MX8-3.3V
TSOP

PCI_AD<0>	A0	DQ0	PCI_AD<24>
PCI_AD<1>	A1	DQ1	PCI_AD<25>
PCI_AD<2>	A2	DQ2	PCI_AD<26>
PCI_AD<3>	A3	DQ3	PCI_AD<27>
PCI_AD<4>	A4	DQ4	PCI_AD<28>
PCI_AD<5>	A5	DQ5	PCI_AD<29>
PCI_AD<6>	A6	DQ6	PCI_AD<30>
PCI_AD<7>	A7	DQ7	PCI_AD<31>
PCI_AD<8>	A8		
PCI_AD<9>	A9		
PCI_AD<10>	A10		
PCI_AD<11>	A11		
PCI_AD<12>	A12		
PCI_AD<13>	A13		
PCI_AD<14>	A14		
PCI_AD<15>	A15		
PCI_AD<16>	A16		
PCI_AD<17>	A17		
PCI_AD<18>	A18		
PCI_AD<19>	A19		
PCI_AD<20>	A20		
ROM_ONBOARD_CS_L	CE		
ROM_OE_L	OE		
ROM_RW_L	WE		
ROM_WP_L	WP		
INT_RESET_L	PWD		
	GND		

+3V_MAIN
R691 10K 5% 1/16W MF 402
R112 10K 5% 1/16W MF 402
R674 1K 5% 1/16W MF 402
ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

Weak pulldowns ensure CKEs stay low
after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0>
RAM_CKE<1>
RAM_CKE<2>
RAM_CKE<3>

INT_2_5V_COLD	R247 10K 5% 1/16W MF 402	RAM_CKE<0>	
INT_2_5V_COLD	R257 10K 5% 1/16W MF 402	RAM_CKE<1>	
INT_2_5V_COLD	R260 10K 5% 1/16W MF 402	RAM_CKE<2>	
INT_2_5V_COLD	R265 10K 5% 1/16W MF 402	RAM_CKE<3>	

INT - DDR/BOOTROM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

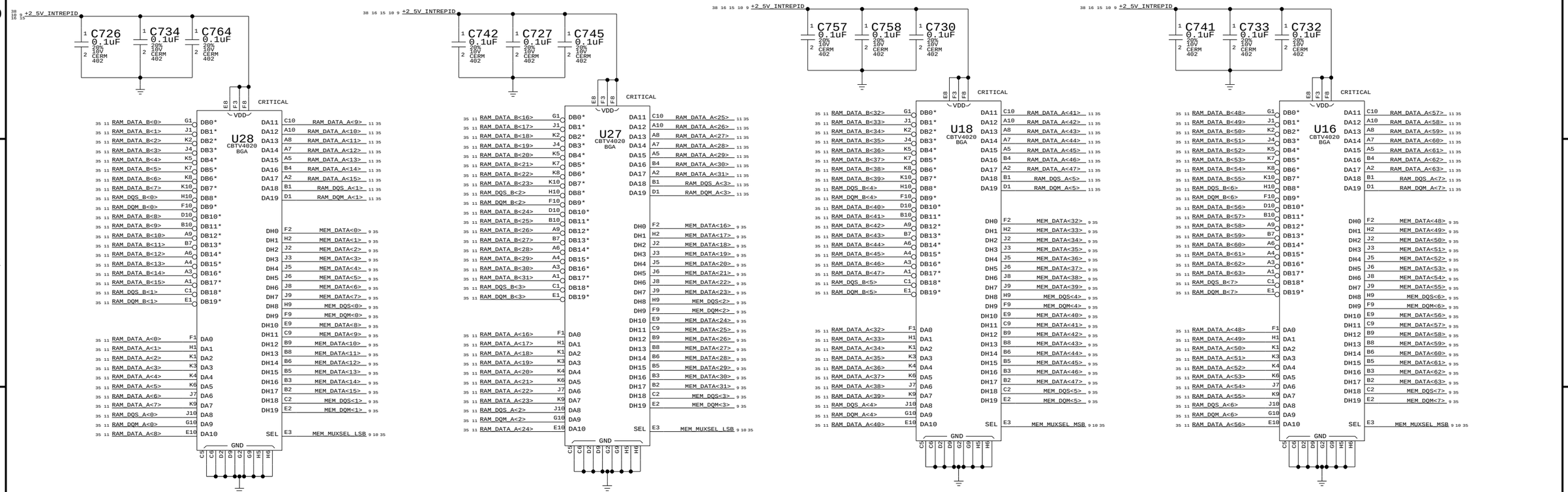
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 9 OF 40	

www.vinafix.vn



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

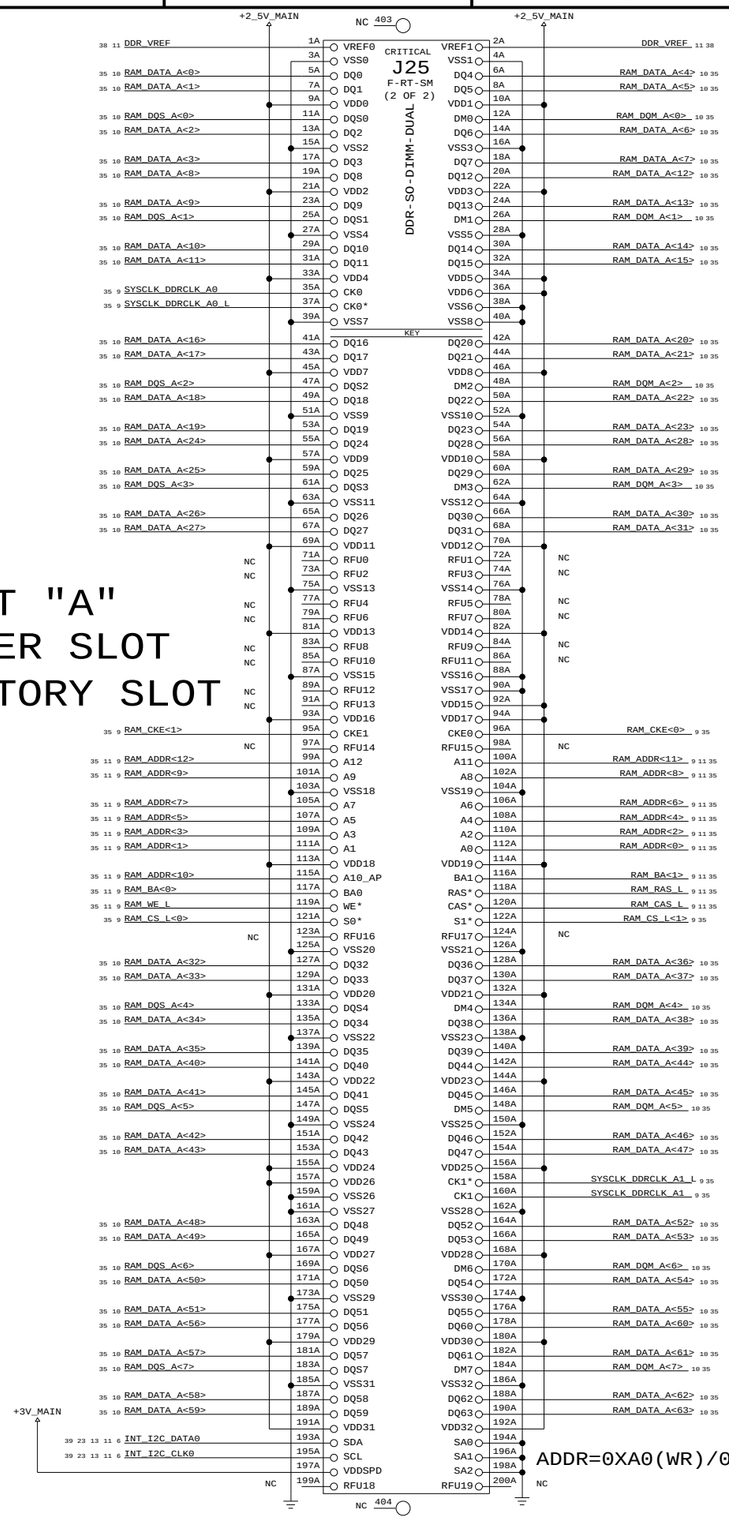
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

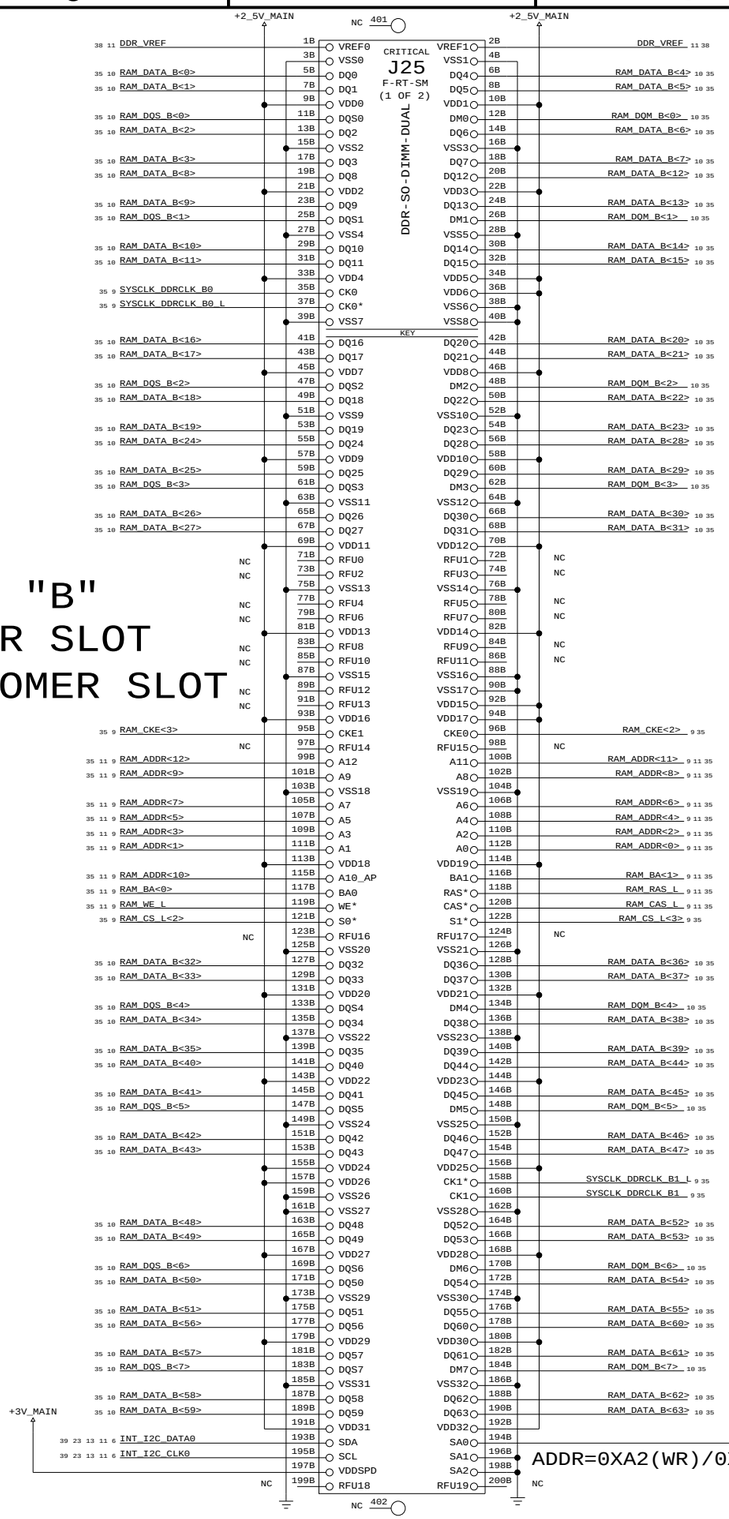
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 10 OF 40	

www.vinafix.vn

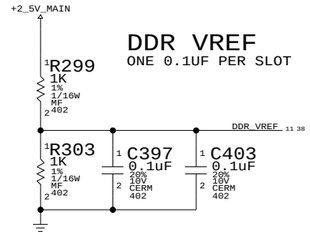


SLOT "A"
LOWER SLOT
FACTORY SLOT

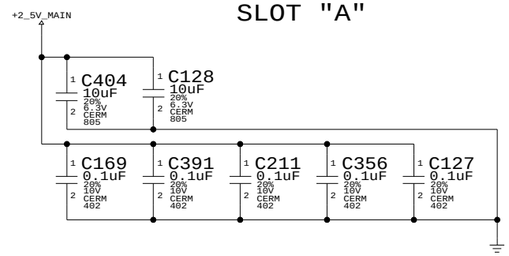


SLOT "B"
UPPER SLOT
CUSTOMER SLOT

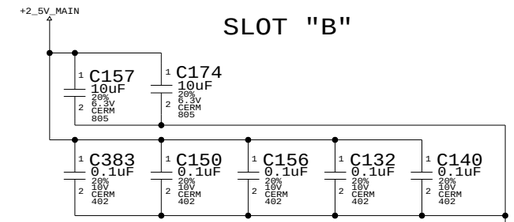
NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting



DDR VREF
ONE 0.1UF PER SLOT



DDR BYPASS
SLOT "A"



SLOT "B"

DDR SODIMM CONNS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

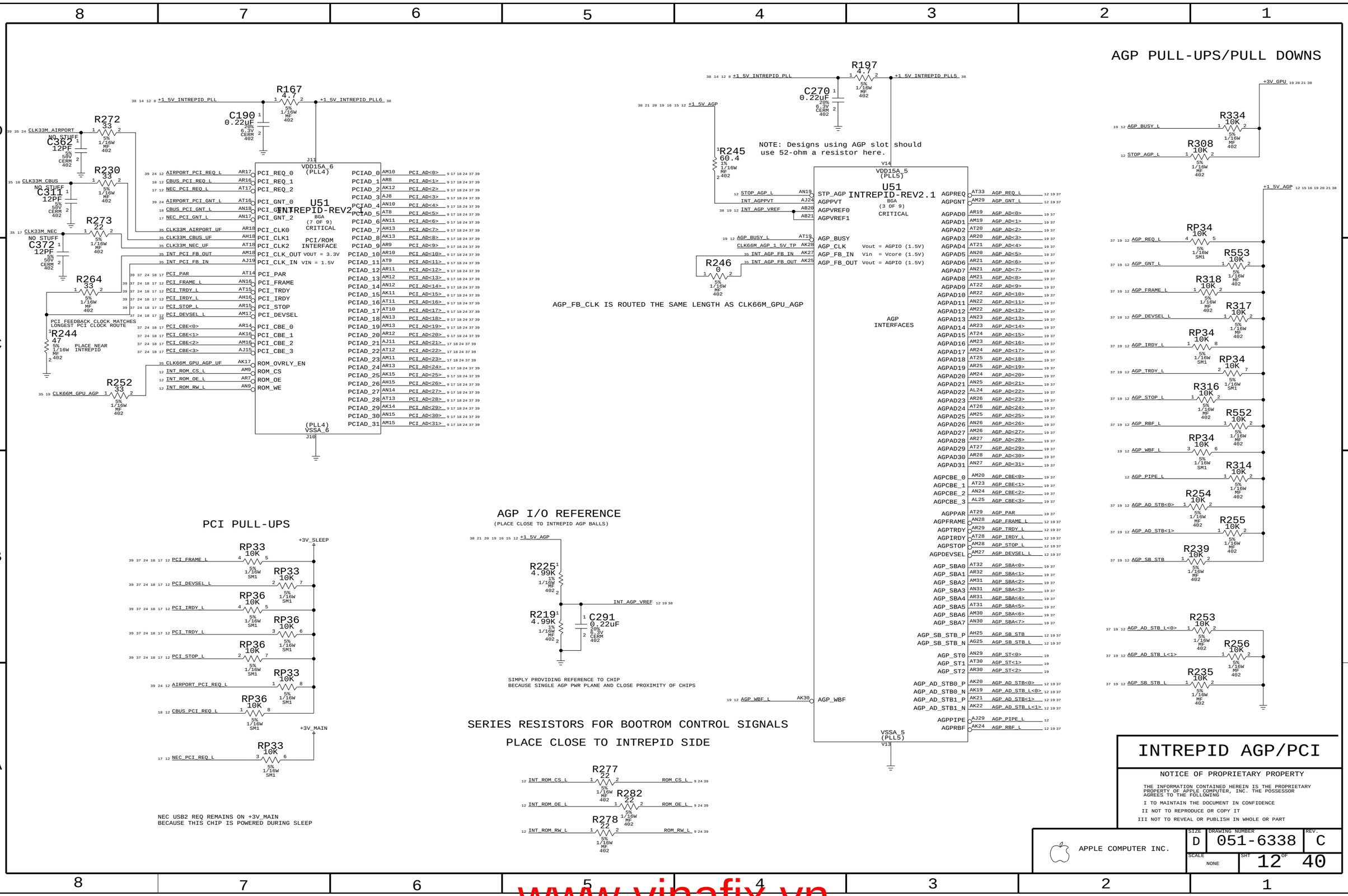
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

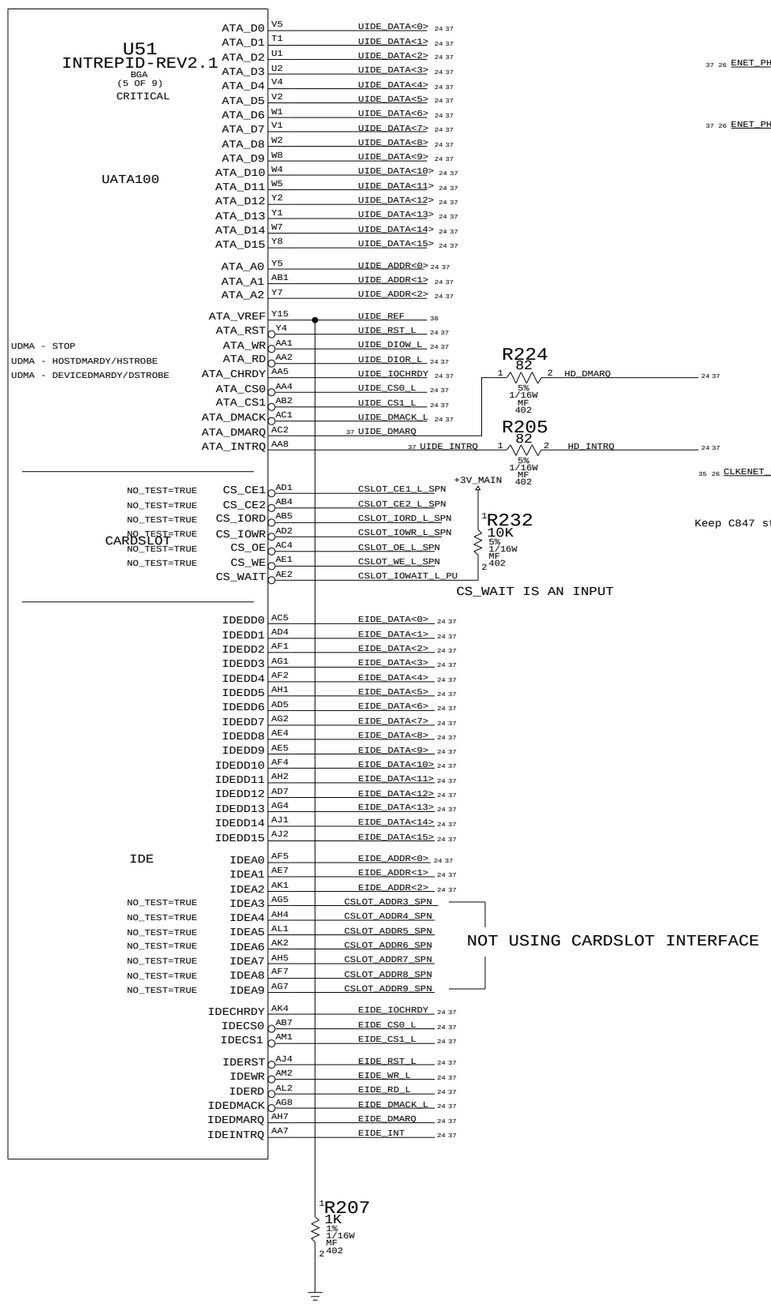
APPLE COMPUTER INC.

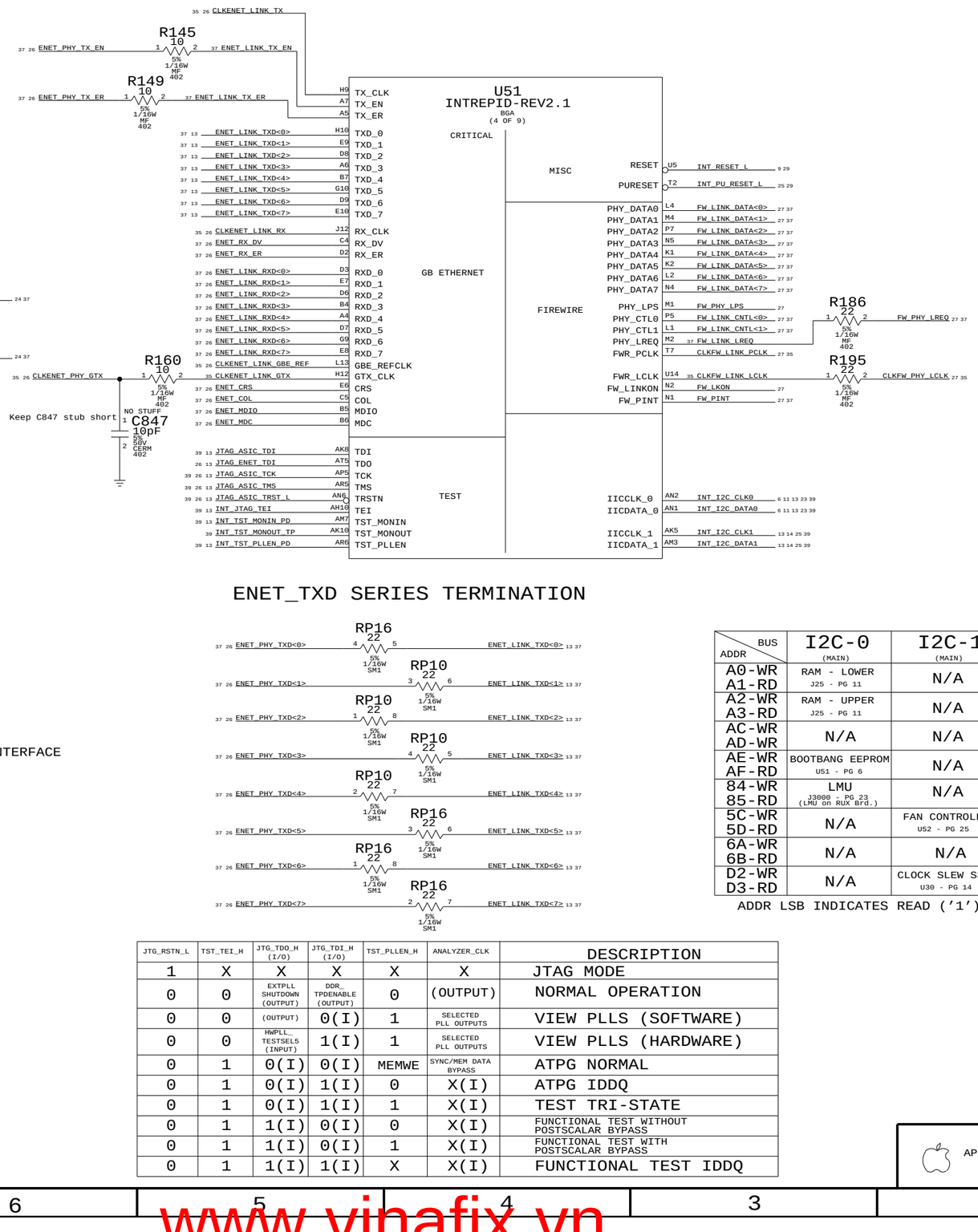
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 11 OF 40	

www.vinafix.vn



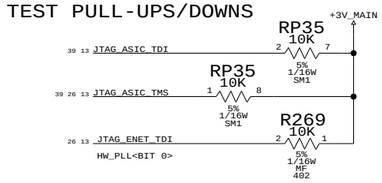
www.vinafix.vn



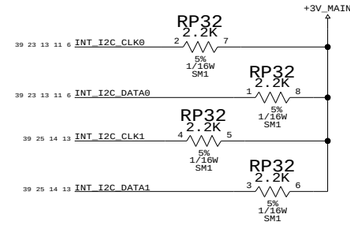


ENET_TXD SERIES TERMINATION

TEST PULL-UPS/DOWNS



I2C PULL-UPS



BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 13 OF 40	

www.vinafix.vn

USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R156 10K — USB_DBM
R157 10K — USB_DBP
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP — BT_USB_DP
R179 22 — USB_DEM — BT_USB_DM
R178 15K
R175 15K

PORT F/MODEM

R192 22 — USB_DFP — MODEM_USB_DP
R188 22 — USB_DFM — MODEM_USB_DM
R189 15K
R193 15K

PCI INTERRUPTS

R148 10K — CBUS_INT_L
R746 10K — AIRPORT_PCI_INT_L
R158 10K — NEC_PCI_INT_L

GPIO/EXTINT PULLUPS

R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP5 10K — INT_EXTINT11_PU
RP6 10K — INT_EXTINT10_PU
RP4 10K — INT_EXTINT12_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K — INT_MOD_DTO_UF
RP15 10K — INT_MOD_CLKOUT_UF
RP15 10K — INT_MOD_DTI
RP15 10K — INT_MOD_SYNC_UF
R206 10K — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

U49 LT1962-ADJ MSOP

R568 0 (NO STUFF) — +2_5V_MAIN
R565 0 — +1_8V_MAIN
LTC1962_INT_VIN
C721 1uF 10V CERM 603
C392 0.01uF 10V CERM 402
R574 18.7K 1% 1/16W MF 402
C723 10uF 6.3V CERM 805
R567 68.1K 1% 1/16W MF 402
LT1962_INT_ADJ
LT1962_INT_BYP
+1_5V_INTREPID_PLL -> 1.55V OUTPUT

U51 INTREPID-REV2.1 BGA (6 OF 9) CRITICAL

R240 4.7 — +1_5V_INTREPID_PLL8
R280 4.7 — +1_5V_INTREPID_PLL4
R279 4.7 — +1_5V_INTREPID_PLL3
R243 4.7 — +1_5V_INTREPID_PLL2
R201 4.7 — +1_5V_INTREPID_PLL1
C337 0.22uF
C389 0.22uF
C388 0.22uF
C386 0.22uF
C387 0.22uF

L13 FERR-EMI-100-OHM SM — +3V_MAIN
+3V_INTREPID_USB
C235 0.01uF 16V CERM 402
C246 0.1uF 10V CERM 402
C256 10uF 6.3V CERM 805

PCI_VDD15A_1 (PLL1) AA16
PCI_VDD15A_2 (PLL2) AJ12
PCI_VDD15A_3 (PLL3) AJ17
PCI_VDD15A_4 (PLL7) AJ18
VDD15A_8 (PLL9) AG29
VDDU33_1 T8
VDDU33_2 U8

GPIO0 — VCORE A/B SEL
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO9
GPIO11
GPIO12
GPIO15
GPIO16
GENERAL PURPOSE I/O'S

EXTINT0
EXTINT1
EXTINT2
EXTINT3
EXTINT4
EXTINT5
EXTINT6
EXTINT7
EXTINT8
EXTINT9
EXTINT10 — CBUS_REG_L
EXTINT11 — CBUS_IREQ_L
EXTINT12
EXTINT13
EXTINT14
EXTINT15
EXTINT16
EXTINT17
CPU_INT
INTERRUPTS
POWERBOOK SPARE

PCIPME
PROCSLEEPREQ
PENDPROCINT

XTAL_IN
XTAL_OUT
STOPXTAL
WATCHDOG
BUF_REF_CLOCK_OUT
SS_REF_CLK_IN
CLOCKS

SCCTXDA AF9 COMM_TXD_L
SCCRTSA AN3 COMM_RTS_L
SCCDTRA AF10 COMM_DTR_L
SCCRXDA AG11 COMM_RXD
SCCGPIOA AG9 COMM_GPIO_L
VIA SCCTRXCA AT4 COMM_TRXC
MISO SCCTXDB AR4 PMU_FROM_INT
REQ* SCCRTSB AL5 PMU_REQ_L
MOSI SCCRXDB AG10 PMU_TO_INT
ACK* SCCGPIOB AP4 PMU_ACK_L
SCK SCCTRXCB AM5 PMU_CLK

USB_VD0_P L8 USB_DAP
USB_VD0_N L7 USB_DAM
USB_VD1_P G2 USB_DBP
USB_VD1_N G1 USB_DBM
USB_PRTPWR0 J4 USB_PWREN_AB_L
USB_PWRFLT0 K4 USB_OC_AB_L
USB_VD2_P H2 USB_DCP
USB_VD2_N H1 USB_DCM
USB_VD3_P M7 USB_DDP
USB_VD3_N M8 USB_DDM
USB_PRTPWR1 J2 USB_PWREN_CD_L
USB_PWRFLT1 J1 USB_OC_CD_L
USB_VD4_P K5 USB_DEP
USB_VD4_N L5 USB_DEM
USB_VD5_P P8 USB_DFP
USB_VD5_N N8 USB_DFM
USB_PRTPWR2 M5 USB_PWREN_EF_L
USB_PWRFLT2 N7 USB_OC_EF_L
USB

AUD_DTO R4 INT_I2S0_SND_TO_DAC_UF
AUD_DTI R7 INT_I2S0_SND_FROM_ADC
AUD_SYNC T5 INT_I2S0_SND_LRCLK_UF
AUD_BITCLK P2 INT_I2S0_SND_SCLK_UF
AUD_CLKOUT R5 INT_I2S0_SND_MCLK_UF
MOD_DTO R2 INT_MOD_DTO_UF
(SIGNAL FROM MODEM) MOD_DTI T4 INT_MOD_DTI
MOD_SYNC R1 INT_MOD_SYNC_UF
MOD_BITCLK V8 INT_MOD_BITCLK_UF
MOD_CLKOUT P1 INT_MOD_CLKOUT_UF
AUDIO/I2S

IICCLK_2 AL4
IICDATA_2 AH8
IIC

VSSA1 (PLL1) AA15
VSSA2 (PLL2) AJ13
VSSA3 (PLL3) AJ16
VSSA4 (PLL7) AK18
VSSA_8 (PLL9) AH29
VSSU_1 R9
VSSU_2 R8

U31 CY28512D TSSOP

CPU0 — CG_CLKOUT1 — INT_REF_CLK_IN
CLKIN
FSEL — CG_FSEL
SCLK — INT_I2C_CLK1
SDATA — INT_I2C_DATA1
ADDRSEL INTERNAL 250K PULL-DOWN
RESET* — CG_RESET_L
PD*
LOCK OPEN DRAIN OUTPUT — CG_LOCK
ODSEL INTERNAL 250K PULL-UP
VDD0 VDD1 VDDA VDDC VDD18
VSS0 VSS1 VSSA VSSC VSSQ
CRITICAL
INTERNAL 250K PULL-UP
OUTPUT IMPEDANCE ~18-20 OHMS

R286 0 (NO STUFF)
R287 10K
R288 10K
R295 10K (NO STUFF)
R293 33
R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT
R284 0 — VCORE_VGATE
R296 10K (NO STUFF)
R142 0 — VCORE_VGATE
MAIN_RESET_L

L15 400-OHM-EMI SM-1 — +3V_MAIN
L14 400-OHM-EMI SM-1 — +2_5V_MAIN
+3V_CG_PLL_MAIN
C400 0.1uF 10V CERM 402
C402 1uF 10V CERM 603
C399 0.1uF 10V CERM 402
C394 0.1uF 10V CERM 402
+2_5V_CG_MAIN

J9 U.FL-R SMT F-ST-SM (NO STUFF)
CLK18M_INT_EXT
R134 0 (NO STUFF)
R113 51
R144 10M (NO STUFF)
R143 0
R218 0
Y2 18.432M CRITICAL 8X4.5MM-SM
C152 22pF 50V CERM 402
C151 22pF 50V CERM 402
CLK18M_XTAL_IN
CLK18M_INT_XOUT
CLK18M_INT_XIN
INT_REF_CLK_OUT
INT_REF_CLK_OUT_UF
INT_REF_CLK_IN
CRYSTAL LOAD CAPACITANCE IS 16PF

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

R258 1K — INT_I2C_CLK2
R241 1K — INT_I2C_DATA2
+3V_SLEEP

INT - USB/GPIOS/I2S

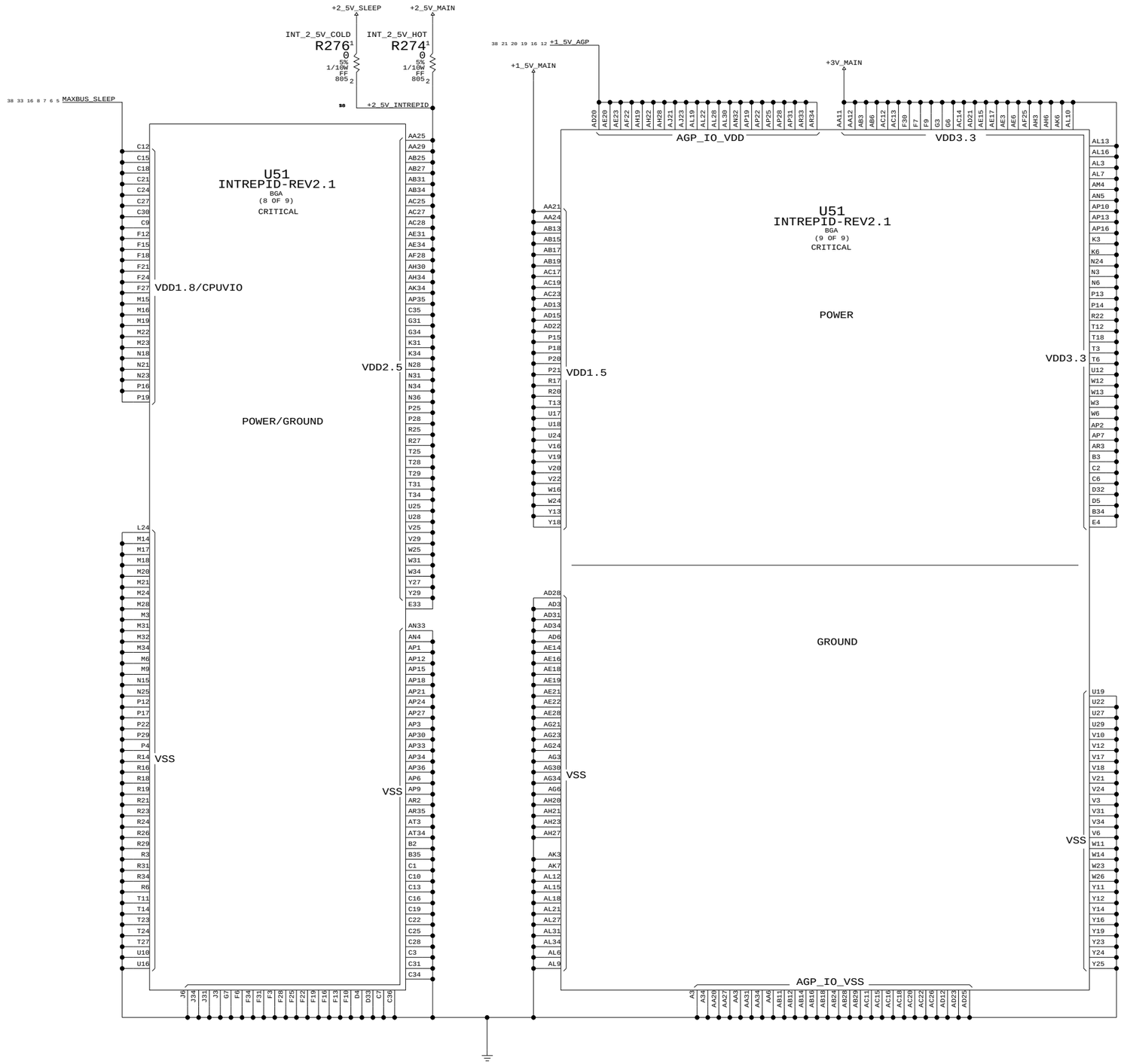
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV. C
SCALE NONE | SHT 14 OF 40

www.vinafix.vn



Intrepid Power

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 15 OF 40	

www.vinafix.vn

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

33 15 8 7 6 5 38 MAXBUS_SLEEP

C148 10uF 20% 6.3V CERM 805 · C142 10uF 20% 6.3V CERM 805 · C144 10uF 20% 6.3V CERM 805 · C146 10uF 20% 6.3V CERM 805

C182 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C164 0.22uF 20% 6.3V CERM 402 · C225 0.22uF 20% 6.3V CERM 402 · C160 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402

C204 0.22uF 20% 6.3V CERM 402 · C166 0.22uF 20% 6.3V CERM 402 · C205 0.22uF 20% 6.3V CERM 402 · C223 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C183 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402

C165 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C147 0.22uF 20% 6.3V CERM 402 · C149 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF 20% 6.3V CERM 805 · C325 10uF 20% 6.3V CERM 805 · C201 10uF 20% 6.3V CERM 805 · C200 10uF 20% 6.3V CERM 805

C299 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C302 0.22uF 20% 6.3V CERM 402 · C300 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C272 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402

C301 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C224 0.22uF 20% 6.3V CERM 402 · C222 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402

C271 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C303 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C258 0.22uF 20% 6.3V CERM 402 · C236 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

38 21 20 19 15 12 +1_5V_AGP

C381 10uF 20% 6.3V CERM 805 · C380 10uF 20% 6.3V CERM 805 · C382 10uF 20% 6.3V CERM 805 · C379 10uF 20% 6.3V CERM 805

C367 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C330 0.22uF 20% 6.3V CERM 402 · C363 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402 · C332 0.22uF 20% 6.3V CERM 402 · C361 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C328 0.22uF 20% 6.3V CERM 402 · C364 0.22uF 20% 6.3V CERM 402

C365 0.22uF 20% 6.3V CERM 402 · C329 0.22uF 20% 6.3V CERM 402 · C345 0.22uF 20% 6.3V CERM 402 · C346 0.22uF 20% 6.3V CERM 402 · C373 0.22uF 20% 6.3V CERM 402 · C344 0.22uF 20% 6.3V CERM 402 · C331 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C347 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF 20% 6.3V CERM 805 · C376 10uF 20% 6.3V CERM 805 · C377 10uF 20% 6.3V CERM 805 · C375 10uF 20% 6.3V CERM 805

C170 0.22uF 20% 6.3V CERM 402 · C358 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C327 0.22uF 20% 6.3V CERM 402 · C342 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402

C175 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C189 0.22uF 20% 6.3V CERM 402 · C167 0.22uF 20% 6.3V CERM 402 · C371 0.22uF 20% 6.3V CERM 402 · C359 0.22uF 20% 6.3V CERM 402

C285 0.22uF 20% 6.3V CERM 402 · C283 0.22uF 20% 6.3V CERM 402 · C269 0.22uF 20% 6.3V CERM 402 · C221 0.22uF 20% 6.3V CERM 402 · C234 0.22uF 20% 6.3V CERM 402 · C247 0.22uF 20% 6.3V CERM 402 · C257 0.22uF 20% 6.3V CERM 402 · C343 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C228 0.22uF 20% 6.3V CERM 402

C360 0.22uF 20% 6.3V CERM 402 · C308 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C341 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

38 15 10 9 +2_5V_INTREPID

C314 10uF 20% 6.3V CERM 805 · C322 10uF 20% 6.3V CERM 805 · C191 10uF 20% 6.3V CERM 805 · C202 10uF 20% 6.3V CERM 805

C304 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C281 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C253 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C348 0.22uF 20% 6.3V CERM 402 · C192 0.22uF 20% 6.3V CERM 402

C306 0.22uF 20% 6.3V CERM 402 · C252 0.22uF 20% 6.3V CERM 402 · C275 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C218 0.22uF 20% 6.3V CERM 402 · C274 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C168 0.22uF 20% 6.3V CERM 402

C265 0.22uF 20% 6.3V CERM 402 · C251 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402 · C254 0.22uF 20% 6.3V CERM 402 · C305 0.22uF 20% 6.3V CERM 402 · C186 0.22uF 20% 6.3V CERM 402 · C219 0.22uF 20% 6.3V CERM 402 · C315 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402

C323 0.22uF 20% 6.3V CERM 402 · C273 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C203 0.22uF 20% 6.3V CERM 402 · C333 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C231 0.22uF 20% 6.3V CERM 402 · C296 0.22uF 20% 6.3V CERM 402

C239 0.22uF 20% 6.3V CERM 402 · C316 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C282 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF 20% 6.3V CERM 402 · C139 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C735 0.22uF 20% 6.3V CERM 402 · C245 0.22uF 20% 6.3V CERM 402 · C736 0.22uF 20% 6.3V CERM 402 · C739 0.22uF 20% 6.3V CERM 402 · C395 0.22uF 20% 6.3V CERM 402 · C374 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C

SCALE	SHT OF
NONE	16 40

www.vinafix.vn

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part

+3V_NEC_VDD 17 38

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

38 NEC_AVDD

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

38 17 +3V_NEC_VDD

Y1's LOAD CAPACITANCE = 16 pF

CRITICAL
Y1 30.0000M 8X4.5MM-SM

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

NEC_XT2_R

R613 36 1% 1/16W MF 402 — NEC_USB_DAM 25 37 39
R612 36 1% 1/16W MF 402 — NEC_USB_DAP 25 37 39
Low/Full/High Speed (External)
R609 36 1% 1/16W MF 402 — NEC_USB_DBM 25 37 39
R610 36 1% 1/16W MF 402 — NEC_USB_DBP 25 37 39
Low/Full/High Speed (External)

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD_PCI, VDD
H10 H12 — AVDD

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

39 37 24 18 12 9 PCI_AD<0>	M5	AD0	
39 37 24 18 12 9 PCI_AD<1>	P5	AD1	
39 37 24 18 12 9 PCI_AD<2>	N5	AD2	
39 37 24 18 12 9 PCI_AD<3>	P4	AD3	
39 37 24 18 12 9 PCI_AD<4>	N4	AD4	
39 37 24 18 12 9 PCI_AD<5>	M3	AD5	
39 37 24 18 12 9 PCI_AD<6>	N3	AD6	
39 37 24 18 12 9 PCI_AD<7>	M1	AD7	
39 37 24 18 12 9 PCI_AD<8>	L2	AD8	
39 37 24 18 12 9 PCI_AD<9>	L1	AD9	
39 37 24 18 12 9 PCI_AD<10>	K2	AD10	
39 37 24 18 12 9 PCI_AD<11>	L3	AD11	
39 37 24 18 12 9 PCI_AD<12>	K1	AD12	
39 37 24 18 12 9 PCI_AD<13>	K3	AD13	
39 37 24 18 12 9 PCI_AD<14>	J2	AD14	
39 37 24 18 12 9 PCI_AD<15>	J1	AD15	
39 37 24 18 12 9 PCI_AD<16>	F2	AD16	
39 37 24 18 12 9 PCI_AD<17>	E3	AD17	
39 37 24 18 12 9 PCI_AD<18>	E1	AD18	
39 37 24 18 12 9 PCI_AD<19>	D3	AD19	
39 37 24 18 12 9 PCI_AD<20>	D1	AD20	
39 37 24 18 12 PCI_AD<21>	D2	AD21	
39 37 24 18 12 PCI_AD<22>	C2	AD22	
39 37 24 18 12 PCI_AD<23>	C1	AD23	
39 37 24 18 12 9 PCI_AD<24>	B4	AD24	
39 37 24 18 12 9 PCI_AD<25>	A4	AD25	
39 37 24 18 12 9 PCI_AD<26>	B5	AD26	
39 37 24 18 12 9 PCI_AD<27>	C4	AD27	
39 37 24 18 12 9 PCI_AD<28>	A5	AD28	
39 37 24 18 12 9 PCI_AD<29>	C5	AD29	
39 37 24 18 12 9 PCI_AD<30>	B6	AD30	
39 37 24 18 12 9 PCI_AD<31>	A6	AD31	
37 24 18 12 PCI_CBE<0>	M2	CBE0	
37 24 18 12 PCI_CBE<1>	J3	CBE1	
37 24 18 12 PCI_CBE<2>	F1	CBE2	
37 24 18 12 PCI_CBE<3>	C3	CBE3	
39 37 24 18 12 PCI_PAR	J4	PAR	
39 37 24 18 12 PCI_FRAME_L	F3	FRAME	
39 37 24 18 12 PCI_IRDY_L	F4	IRDY	
39 37 24 18 12 PCI_TRDY_L	G1	TRDY	
39 37 24 18 12 PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
39 37 24 18 12 PCI_DEVSEL_L	G2	DEVSEL	
12 NEC_PCI_REQ_L	C6	REQ	
12 NEC_PCI_GNT_L	D6	GNT	
18 PCI_PERR_L	H2	PERR	
18 PCI_SERR_L	H1	SERR	OD
NEC_PCI_INTA_L	C7	INTA	OD
NEC_PCI_INTB_L	B7	INTB	OD
NEC_PCI_INTC_L	A7	INTC	OD
35 12 CLK33M_NEC	A8	PCLK	
17 NEC_IO_RESET_L	B8	VBBRST	
NEC_CRUN_L	N6	CRUN	
17 NEC_PME_L	D9	PME	OD
17 NEC_MAIN_RESET_L	C9	VCCRST	
NEC_SMI_L_TP	L6	SMI	OD
17 NEC_LEGC	L7	LEGC	

R636 22 5% 1/16W MF 402

Series Rpaks required to facilitate NAND-tree testing

RP45 47 5% 1/16W SM1
14 NEC_PCI_INT_L

R617 4.7K 5% 1/16W MF 402

RP44 47 5% 1/16W SM1
29 26 23 IO_RESET_L — NEC_IO_RESET_L 17
39 29 24 14 PMU_PME_L — NEC_PME_L 17
39 29 24 19 18 14 MAIN_RESET_L — NEC_MAIN_RESET_L 17
17 NEC_LEGC

VSS
B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

XT1/SCLK	L9	NEC_XT1
XT2	P8	NEC_XT2
RSDM1	M14	NEC_USB_RSDM1
DM1	M13	(NEC_USB_DAM)
DP1	L14	(NEC_USB_DAP)
RSDP1	K13	NEC_USB_RSDP1
RSDM2	K14	NEC_USB_RSDM2
DM2	K12	(NEC_USB_DBM)
DP2	J14	(NEC_USB_DBP)
RSDP2	J12	NEC_USB_RSDP2
RSDM3	H11	NC
DM3	G11	
DP3	G13	
RSDP3	G14	NC
RSDM4	F12	NC
DM4	F14	
DP4	E12	
RSDP4	E14	NC
RSDM5	E13	NC
DM5	D14	
DP5	C13	
RSDP5	C14	NC
RREF	P11	NEC_RREF

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11 — NEC_AVSS_F 17

OCI1	B12	NEC_LUSB_OCI 17
OCI2	B11	NEC_RUSB_OCI 17
OCI3	B10	NEC_OCI<3>
OCI4	A10	NEC_OCI<4>
OCI5	B9	NEC_OCI<5>
PPON1	C12 OUT	NEC_LUSB_PPON 25 39
PPON2	A11 OUT	NEC_RUSB_PPON 25 39
PPON3	C11 OUT	NEC_PPON3_TP
PPON4	C10 OUT	NEC_PPON4_TP
PPON5	A9 OUT	NEC_PPON5_TP
NC1	P6	NEC_NC<1>
NC2	M6	NEC_NC<2>

RP43 10K 5% 1/16W SM1 — +3V_NEC_VDD 17 38
RP43 10K 5% 1/16W SM1
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

NEC documentation indicates that NCs must be tied high.

NTEST1	M8 IPD	NC
SMC	M7 IPD	NC
TEB	N7 IPD	NC
AMC	P7 IPD	NEC_AMC_TP
TEST	L8 IPD	NC
NANDTEST	M10	NEC_NANDTESTEN_TP
SRCLK	M9	NC
SRDTA	N9	NEC_NANDTESTOUT_TP
SRMOD	P9 IPD	NC
AVSS		
AVSS(R)	N11 P13 M12	

R798 0 5% 1/16W MF 603 — 17 NEC_AVSS_F

+3V_MAIN

RP43 10K 5% 1/16W SM1
RP43 10K 5% 1/16W SM1
R607 0 5% 1/16W MF 402 — 17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 25 39
R608 0 5% 1/16W MF 402 — 17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 25 39

NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 17 OF 40	

www.vinafix.vn

PCI1510 PULL-UPS

+3V_SLEEP

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)

R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)

R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805

C786 0.22uF 20% 6.3V CERM 402

C60 10uF 20% 6.3V CERM 805

C776 10uF 20% 6.3V CERM 805

C789 0.22uF 20% 6.3V CERM 402

C791 0.22uF 20% 6.3V CERM 402

C784 0.22uF 20% 6.3V CERM 402

C782 0.22uF 20% 6.3V CERM 402

C783 0.22uF 20% 6.3V CERM 402

C778 0.22uF 20% 6.3V CERM 402

C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

R719 22 5% 1/16W MF 402

R723 47 5% 1/16W MF 402 — MAIN_RESET_L (29 24 19 17 14)

RP1 10K 5% 1/32W 25V (SM)
- CBUS_MFUNC1_PD (18)
- CBUS_MFUNC2_PD (18)
- CBUS_MFUNC3_PD (18)
- CBUS_MFUNC4_PD (18)
- CBUS_MFUNC5_PD (18)
- CBUS_MFUNC6_PD (18)

U8 PCI1510GGU (BGA)

NC	H10	CLK_48_RSVD/NC
PCI1510_VR_EN_L	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0> (39 37 24 17 12 9)	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
(PCI_AD<19>)	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	IRDY
PCI_SERR_L (18 17)	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
PCI_PERR_L (18 17)	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L (12)	C2	REQ
CBUS_PCI_GNT_L (12)	C1	GNT
CLK33M_CBUS (35 12)	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU (18)	N10	SUSPEND
CBUS_INT_L (14)	K7	MFUNC0
CBUS_MFUNC1_PD (18)	N9	MFUNC1
CBUS_MFUNC2_PD (18)	L9	MFUNC2
CBUS_MFUNC3_PD (18)	K10	MFUNC3
CBUS_MFUNC4_PD (18)	M10	MFUNC4
CBUS_MFUNC5_PD (18)	N12	MFUNC5
CBUS_MFUNC6_PD (18)	L10	MFUNC6
	L11	GRST

CRITICAL — CLAMP FOR PC-CARD, CLAMP FOR PCI

	B11	VCCCB
	L3	VCCP
CBUS_VCCD0_L	N13	VCCD0*
CBUS_VCCD1_L	L12	VCCD1*
CBUS_VPPD0	K9	VPPD0
CBUS_VPPD1	M11	VPPD1
CBUS_DET_1_L (18 39)	L13	CD1*/CCD1*
CBUS_DET_2_L (18 39)	B5	CD2*/CCD2*
CBUS_IORD_L (18)	F12	IORD*/CAD13
CBUS_IOWR_L (18)	C11	IOWR*/CAD15
CBUS_OE_L (18)	G10	OE*/CAD11
CBUS_CE1_L (18)	H13	CE1*/CC/BE0*
CBUS_VS1 (18)	B2	VS1*/CVS1
CBUS_VS2 (18)	A9	VS2*/CVS2
CBUS_WE_L (18)	D13	WE*/CGNT*
CBUS_READY (18)	A6	RDY/IREQ*/CINT*
CBUS_RESET_L (18)	D8	RESET/CRST*
CBUS_REG_L (18)	A8	REG*/CC/BE3*
CBUS_BVD1_L (18)	C6	BVD1/CSTSCHG/STSCHG*/RI*
CBUS_BVD2_L (18)	D6	BVD2/SPKR*/CAUDIO
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*
CBUS_CE2_L (18)	G13	CE2/CAD10*
CBUS_INPACK_L (18)	B8	INPACK/CREQ*
CBUS_WAIT_L (18)	B6	WAIT/CSERR*
CBUS_ADDR<0> (18)	C7	A0/CAD26
CBUS_ADDR<1> (18)	D7	A1/CAD25
CBUS_ADDR<2> (18)	B7	A2/CAD24
CBUS_ADDR<3> (18)	D10	A3/CAD23
CBUS_ADDR<4> (18)	B12	A4/CAD22
CBUS_ADDR<5> (18)	C8	A5/CAD21
CBUS_ADDR<6> (18)	C9	A6/CAD20
CBUS_ADDR<7> (18)	A12	A7/CAD18
CBUS_ADDR<8> (18)	E11	A8/CC/BE1*
CBUS_ADDR<9> (18)	F11	A9/CAD14
CBUS_ADDR<10> (18)	G11	A10/CAD9
CBUS_ADDR<11> (18)	G12	A11/CAD12
CBUS_ADDR<12> (18)	D9	A12/CC/BE2*
CBUS_ADDR<13> (18)	E12	A13/CPAR
CBUS_ADDR<14> (18)	D12	A14/CPERR*
CBUS_ADDR<15> (18)	C10	A15/CIRDY*
CBUS_ADDR_16_UF	B13	A16/CCLK
CBUS_ADDR<17> (18)	F10	A17/CAD16
CBUS_ADDR<18> (18)	E13	A18/RSVD
CBUS_ADDR<19> (18)	A13	A19/CBLOCK*
CBUS_ADDR<20> (18)	E10	A20/CSTOP*
CBUS_ADDR<21> (18)	D11	A21/CDEVSEL*
CBUS_ADDR<22> (18)	C12	A22/CTRDY*
CBUS_ADDR<23> (18)	A10	A23/CFRAME*
CBUS_ADDR<24> (18)	B10	A24/CAD17
CBUS_ADDR<25> (18)	B9	A25/CAD19
CBUS_DATA<0> (18)	A4	D0/CAD27
CBUS_DATA<1> (18)	C4	D1/CAD29
CBUS_DATA<2> (18)	A3	D2/RSVD
CBUS_DATA<3> (18)	K11	D3/CAD0
CBUS_DATA<4> (18)	K12	D4/CAD1
CBUS_DATA<5> (18)	J13	D5/CAD3
CBUS_DATA<6> (18)	J10	D6/CAD5
CBUS_DATA<7> (18)	H12	D7/CAD7
CBUS_DATA<8> (18)	C5	D8/CAD28
CBUS_DATA<9> (18)	B4	D9/CAD30
CBUS_DATA<10> (18)	B3	D10/CAD31
CBUS_DATA<11> (18)	M12	D11/CAD2
CBUS_DATA<12> (18)	J11	D12/CAD4
CBUS_DATA<13> (18)	K13	D13/CAD6
CBUS_DATA<14> (18)	J12	D14/RSVD
CBUS_DATA<15> (18)	H11	D15/CAD8

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

GND: A2 A11 D1 F13 H4 K8 M13 N2

+3V_MAIN

+5V_MAIN

R726 0 5% 1/16W MF 402 — SLEEP_L_LS5 (26 34 29 33 32)

TPS2211_SHTDWN_L

U4 TPS2211 SSOI

NC	9	
V_12	5	
V_5_1	6	
V_5_2	3	AVPP
V_3_1	4	AVCC0
V_3_2	1	AVCC1
VCCD0	2	AVCC2
VCCD1	15	
VPPD0	14	
VPPD1	16	
SHTDWN	7	
GND		OC (8 NC)
	10	+VPP_CBUS_SW (18 38)
	11	+VCC_CBUS_SW (18 38)
	12	
	13	

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

C40 0.1uF 20% 10V CERM 402

C37 0.1uF 20% 10V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 16V CERM 805

C800 2.2uF 20% 16V CERM 805

PC CARD/CARDBUS CONNECTOR

CRITICAL

J5 QT500806-L111 M-ST-SM1

	84	81	
	2	1	CBUS_DATA<3> (18)
CBUS_DET_1_L (39 18)	4	3	CBUS_DATA<4> (18)
CBUS_DATA<11> (18)	6	5	CBUS_DATA<5> (18)
CBUS_DATA<12> (18)	8	7	CBUS_DATA<6> (18)
CBUS_DATA<13> (18)	10	9	
	12	11	CBUS_DATA<7> (18)
CBUS_DATA<14> (18)	14	13	CBUS_CE1_L (18)
CBUS_DATA<15> (18)	16	15	CBUS_ADDR<10> (18)
CBUS_CE2_L (18)	18	17	CBUS_OE_L (18)
CBUS_VS1 (18)	20	19	
	22	21	CBUS_ADDR<11> (18)
CBUS_IORD_L (18)	24	23	CBUS_ADDR<9> (18)
CBUS_IOWR_L (18)	26	25	CBUS_ADDR<8> (18)
CBUS_ADDR<17> (18)	28	27	CBUS_ADDR<13> (18)
CBUS_ADDR<18> (18)	30	29	
	32	31	CBUS_ADDR<14> (18)
CBUS_ADDR<19> (18)	34	33	CBUS_WE_L (18)
CBUS_ADDR<20> (18)	36	35	CBUS_READY (18)
CBUS_ADDR<21> (18)	38	37	+VCC_CBUS_SW (18 38)
+VCC_CBUS_SW (38 18)	40	39	
	42	41	+VPP_CBUS_SW (18 38)
+VPP_CBUS_SW (38 18)	44	43	CBUS_ADDR<16> (18)
CBUS_ADDR<22> (18)	46	45	CBUS_ADDR<15> (18)
CBUS_ADDR<23> (18)	48	47	CBUS_ADDR<12> (18)
CBUS_ADDR<24> (18)	50	49	
	52	51	CBUS_ADDR<7> (18)
CBUS_ADDR<25> (18)	54	53	CBUS_ADDR<6> (18)
CBUS_VS2 (18)	56	55	CBUS_ADDR<5> (18)
CBUS_RESET_L (18)	58	57	CBUS_ADDR<4> (18)
CBUS_WAIT_L (18)	60	59	
	62	61	CBUS_ADDR<3> (18)
CBUS_INPACK_L (18)	64	63	CBUS_ADDR<2> (18)
CBUS_REG_L (18)	66	65	CBUS_ADDR<1> (18)
CBUS_BVD2_L (18)	68	67	CBUS_ADDR<0> (18)
CBUS_BVD1_L (18)	70	69	
	72	71	CBUS_DATA<0> (18)
CBUS_DATA<8> (18)	74	73	CBUS_DATA<1> (18)
CBUS_DATA<9> (18)	76	75	CBUS_DATA<2> (18)
CBUS_DATA<10> (18)	78	77	CBUS_WP_L (18)
CBUS_DET_2_L (39 18)	80	79	
	83	82	

CARDBUS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 18 OF 40	

www.vinafix.vn

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

L22 60-OHM-EMI
C476 0.01uF 20% 16V CERM 402
C457 0.01uF 20% 16V CERM 402
C458 10uF 20% 6.3V CERM 805
C490 0.01uF 20% 16V CERM 402
C442 0.01uF 20% 16V CERM 402
C530 0.01uF 20% 16V CERM 402
GPU_VCORE
GPU_VCORE_VDDCI
+3V_GPU
+1_5V_AGP
R323 10K 5% 1/16W MF 402
R313 47 1% 1/16W MF 402
R338 20K 5% 1/16W MF 402
C412 0.01uF 20% 16V CERM 402
C408 0.1uF 20% 10V CERM 402
(PLACE C408 CLOSE TO AGPREF PIN)

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (6 OF 6)
VSS
VDDCI
GPU_VCORE_VDDCI

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (1 OF 6)

AGP_AD<31:0> AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0
AGP_CBE<3:0> CBEB3 CBEB2 CBEB1 CBEB0
CLK66M_GPU_AGP PCICLK
AGP_FRAME_L FRAMEB
AGP_IRDY_L IRDYB
AGP_TRDY_L TRDYB
AGP_STOP_L STOPB
AGP_DEVSEL_L DEVSELB
AGP_PAR PAR
AGP_REQ_L REQB
AGP_GNT_L GNTB
AGP_ATI_INT_L INTAB
AGP_ATI_RESET_L RSTB
AGP_WBF_L WBF
AGP_ATI_VREFG VREFG
AGP_ATI_VREF VREF

AD_STB0 AGP_AD_STB<0>
AD_STB1 AGP_AD_STB<1>
AD_STBB0 AGP_AD_STB_L<0>
AD_STBB1 AGP_AD_STB_L<1>
AGP_BUSYB AGP_BUSY_L
AGPREF INT_AGP_VREF
AGPTEST GPU_AGP_TEST
AGP8X_DETB AGP8X_DET_PU
SUS_STAT AGP_SUS_STAT_L_PU
ST0 AGP_ST<0>
ST1 AGP_ST<1>
ST2 AGP_ST<2>
SBA7 AGP_SBA<7>
SBA6 AGP_SBA<6>
SBA5 AGP_SBA<5>
SBA4 AGP_SBA<4>
SBA3 AGP_SBA<3>
SBA2 AGP_SBA<2>
SBA1 AGP_SBA<1>
SBA0 AGP_SBA<0>
RBFB AGP_RBF_L
STP_AGPB AGP_STP_L
SB_STB AGP_SB_STB
SB_STBS AGP_SB_STB_L
RSTB_MSK ATI_RSTB_MSK
DBI_LO ATI_DBI_LO_PU
DBI_HI ATI_DBI_HI_PU

R336 0 5% 1/16W MF 402
R335 20K 5% 1/16W MF 402
+3V_GPU

R337 10K 5% 1/16W MF 402
MAIN_RESET_L IS TOGGLED FOR SLEEP
R309 47 5% 1/16W MF 402
R388 1K 1% 1/16W MF 402
R397 1K 1% 1/16W MF 402
GPU_MEM_IO
R373 1K 1% 1/16W MF 402
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN
R365 1K 1% 1/16W MF 402
C516 0.1uF 20% 10V CERM 402
C508 10uF 20% 6.3V CERM 805

R325 47K 5% 1/16W MF 402
R324 47K 5% 1/16W MF 402
R372 45.3 1% 1/16W MF 402

R370 4.7K 5% 1/16W MF 402
R371 4.7K 5% 1/16W MF 402
R375 4.7K 5% 1/16W MF 402
R376 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO
ATI_MEMIO_HI
ATI_MEMVMODE0
ATI_MEMVMODE1
MEMVMODE0
MEMVMODE1
+1_8V_GPU

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

TEST_YCLK
TEST_MLCK
MEMTEST
PLLTEST
GPU_THERM_DP
GPU_THERM_DM
GPU_MEM_IO
(PULL-UP to GPU_MEM_IO)
ATI_MEMTEST

CRITICAL
U47 RAGE_MOBILITY M10-CSP64 64MB BGA (2 OF 6)
VSS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

+3V_SLEEP
L78 400-OHM-EMI
L79 400-OHM-EMI
L80 400-OHM-EMI
C856 10uF 20% 6.3V CERM 805
C858 100pF 5% 50V CERM 402
C860 100pF 5% 50V CERM 402
C854 10uF 20% 6.3V CERM 805
C855 10uF 20% 6.3V CERM 805
C857 100pF 5% 50V CERM 402
C859 100pF 5% 50V CERM 402
C861 100pF 5% 50V CERM 402
C862 100pF 5% 50V CERM 402
C863 10uF 20% 6.3V CERM 805
+3V_SI_AVCC
+3V_SI_PLLVCC
+3V_SI_VCC
PLL NOISE SHOULD BE LESS THAN 100mV PEAK-TO-PEAK

MAIN_RESET_L
R832 47 5% 1/16W MF 402
R833 47 5% 1/16W MF 402
R835 10K 5% 1/16W MF 402
R818 10K 5% 1/16W MF 402
R823 10K 5% 1/16W MF 402
R825 10K 5% 1/16W MF 402
R837 4.99K 1% 1/16W MF 402
R826 330 5% 1/16W MF 402
R819 10K 5% 1/16W MF 402
R824 10K 5% 1/16W MF 402
R836 10K 5% 1/16W MF 402
NO STUFF

SI_I2C_CLK
SI_I2S_DATA
SI_A2
SI_RST_L
SI_PD_L
SI_HPD
MSEN
SI_MSEN

U58 SIL1162 TSSOP
SCL/DK1
SDA/DK0
CTL3/A2
ISEL/RST*
PD*
EDGE/HTPLG
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11
DE HSYNC VSYNC IDCK+ IDCK-
PGND PGND AGND AGND AGND AGND GND GND THRML PAD
PVCC1 PVCC2 AVCC AVCC AVCC VCC VCC

TXC+ TXC- TX0+ TX0- TX1+ TX1- TX2+ TX2-
SI_TMDS_CLKP SI_TMDS_CLKN SI_TMDS_DP<0> SI_TMDS_DN<0> SI_TMDS_DP<2> SI_TMDS_DP<1> SI_TMDS_DN<1> SI_TMDS_DP<2> SI_TMDS_DN<2>

EXT_SWING
VREF
SI_EXT_SWING_SET
SI_VREF_IDCK_N
(SET TO LOW SWING MODE)
Place C879 close to SI pin#2

RP49 0K EXT_TMDS
RP50 0K EXT_TMDS
RP51 0K EXT_TMDS
RP60 0K EXT_TMDS
ATI_DVOD<1:0>
ATI_DVOD<3:2>
ATI_DVOD<5:4>
ATI_DVOD<7:6>
ATI_DVOD<11:10>
ATI_DVOD<9:8>
GPU_DVOD<1:0>
GPU_DVOD<3:2>
GPU_DVOD<5:4>
GPU_DVOD<7:6>
GPU_DVOD<11:10>
GPU_DVOD<9:8>
ATI_DVO_HSYNC
ATI_DVO_VSYNC
ATI_DVOD_DE
ATI_DVO_CLKP
GPU_DVO_HSYNC
GPU_DVO_VSYNC
GPU_DVOD_DE
GPU_DVO_CLKP

C879 0.1uF 20% 10V CERM 402
R838 1K 1% 1/16W MF 402
R839 1K 1% 1/16W MF 402

R827 300 5% 1/16W MF 402
R828 300 5% 1/16W MF 402
R829 300 5% 1/16W MF 402
R830 300 5% 1/16W MF 402
C865 0.1uF 20% 10V CERM 402
C875 470pF 10% 50V CERM 402
C877 470pF 10% 50V CERM 402
C864 0.1uF 20% 10V CERM 402
C871 470pF 10% 50V CERM 402
C873 470pF 10% 50V CERM 402
C866 0.1uF 20% 10V CERM 402
C876 470pF 10% 50V CERM 402
C878 470pF 10% 50V CERM 402
C867 0.1uF 20% 10V CERM 402
C872 470pF 10% 50V CERM 402
C974 470pF 10% 50V CERM 402
SI_TMDS_CLK_STM
SI_TMDS_D0_STM
SI_TMDS_D1_STM
SI_TMDS_D2_STM
TMDS_CLKP TMDS_CLKN TMDS_DP<0> TMDS_DN<0> TMDS_DP<1> TMDS_DN<1> TMDS_DP<2> TMDS_DN<2>

RP56 22 5% 1/16W SM1
RP52 22 5% 1/16W SM1
RP57 22 5% 1/16W SM1
RP53 22 5% 1/16W SM1
RP58 0 5% 1/16W SM1
RP54 0 5% 1/16W SM1
RP59 0 5% 1/16W SM1
RP55 0 5% 1/16W SM1

27M OSC
(PLACE THE OSCILLATOR AND R304 AND R305 CLOSE TO ATI PIN AJ29)
L16 FERR-EMI-100-OHM
R304 100K 5% 1/16W MF 402
C409 0.1uF 20% 10V CERM 402
C401 4.7uF 20% 6.3V CERM 805
VCC G1 27MHZ OSC SM OE OUT GND
ATI_OSC_OE
ATI_OSC_SLEEP
ATI_CLK27M_OSC
ATI_CLK27M_OSC_SS
R305 0 5% 1/16W MF 402
R315 287 1% 1/16W MF 402
(PLACE R315 CLOSE TO OSC)
R320 162 1% 1/16W MF 402
ATI_CLK27M_IN

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD
L66 FERR-EMI-100-OHM
C384 10uF 20% 6.3V CERM 805
C390 0.1uF 20% 10V CERM 402
VDD U30 CY25811 SOT XIN/CLKIN XOUT SSCLK FRSEL S1 S0 VSS
CY25811_S1
CY25811_S0
R289 0 5% 1/16W MF 402
R297 0 5% 1/16W MF 402
R290 0 5% 1/16W MF 402
R298 0 5% 1/16W MF 402
R285 33 5% 1/16W MF 402
ATI_SSCLK_UF
ATI_SSCLK_IN

M10 AGP INTERFACE

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 19 OF 40	

www.vinafix.vn

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 162 1% 1/16W MF 402 — GPU_TMDS_CLK#
R377 162 1% 1/16W MF 402 — GPU_TMDS_CLK
C536 470pF 10% 50V CERM 402
C522 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 162 1% 1/16W MF 402 — GPU_TMDS_D0#
R369 162 1% 1/16W MF 402 — GPU_TMDS_D0
C515 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402

GPU_TMDS_D1_CMF
R362 162 1% 1/16W MF 402 — GPU_TMDS_D1#
R355 162 1% 1/16W MF 402 — GPU_TMDS_D1
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402

GPU_TMDS_D2_CMF
R350 162 1% 1/16W MF 402 — GPU_TMDS_D2#
R340 162 1% 1/16W MF 402 — GPU_TMDS_D2
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402

R765 10 5% 1/16W MF 402 — GPU_TMDS_CLK#
R767 10 5% 1/16W MF 402 — GPU_TMDS_CLK
R760 10 5% 1/16W MF 402 — GPU_TMDS_D0#
R762 10 5% 1/16W MF 402 — GPU_TMDS_D0
R764 10 5% 1/16W MF 402 — GPU_TMDS_D1#
R766 10 5% 1/16W MF 402 — GPU_TMDS_D1
R761 10 5% 1/16W MF 402 — GPU_TMDS_D2#
R763 10 5% 1/16W MF 402 — GPU_TMDS_D2

Place all TMDS 10 ohms close to GPU

R389 10K 5% 1/16W MF 402 — +1_8V_GPU
R840 10K 5% 1/16W MF 402 — +3V_GPU
ZV_LCDDATA20_PU

R378 1K 5% 1/16W MF 402

R380 10K 5% 1/16W MF 402 — NO STUFF — +3V_GPU
HPD_PWR_SNS_EN
GPU_VCORE_CNTL_L

R351 1K 5% 1/16W MF 402 — ATI_TESTEN

CRITICAL
U47
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

ATI_DVOD<0>	AJ5	ZV_LCDDATA0
ATI_DVOD<1>	AK5	ZV_LCDDATA1
ATI_DVOD<2>	AG6	ZV_LCDDATA2
ATI_DVOD<3>	AH6	ZV_LCDDATA3
ATI_DVOD<4>	AJ6	ZV_LCDDATA4
ATI_DVOD<5>	AK6	ZV_LCDDATA5
ATI_DVOD<6>	AG7	ZV_LCDDATA6
ATI_DVOD<7>	AH7	ZV_LCDDATA7
ATI_DVOD<8>	AJ7	ZV_LCDDATA8
ATI_DVOD<9>	AK7	ZV_LCDDATA9
ATI_DVOD<10>	AG8	ZV_LCDDATA10
ATI_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
ATI_DVO_VSYNC	AJ4	ZV_LCDCNTL0
ATI_DVO_HSYNC	AK4	ZV_LCDCNTL1
ATI_DVOD_DE	AH5	ZV_LCDCNTL2
ATI_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN	AF3	GPIO9
ATI_GPIO10_SPN	AG2	GPIO10
ATI_GPIO11_SPN	AF2	GPIO11
ATI_GPIO12_SPN	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
	AE2	GPIO14
ATI_SSCLK_IN	AE1	GPIO15
	M1	GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

CRITICAL
Q23
SI3446DV
TSOP

L17
FERR-220-OHM
0805

+1_5V_AGP → +1_5V_SLEEP_NECK1
+1_8V_ATI_PVDD → +1_8V_PVDD_NECK
GPU_VCORE → GPU_VCORE_NECK
+GPU_VDD15_UF → +GPU_VDD15_NECK
GPU_CORE_OK

C407 1000pF 10% 25V X7R 402

R346 75 1% 1/16W MF 402 — NO STUFF
R342 75 1% 1/16W MF 402 — NO STUFF
R341 75 1% 1/16W MF 402 — NO STUFF

R359 75 1% 1/16W MF 402
R356 75 1% 1/16W MF 402
R360 75 1% 1/16W MF 402
R332 715 1% 1/16W MF 402
R333 499 1% 1/16W MF 402

R779 10K 5% 1/16W MF 402 — +3V_GPU
R366 10K 5% 1/16W MF 402
R368 10K 5% 1/16W MF 402

XW11 SM — DP5 BAS16TW SOT-363 — +2_5V_SLEEP_NECK1 → +2_5V_SLEEP
XW12 SM — DP5 BAS16TW SOT-363 — +1_5V_AGP_NECK
XW5 SM — DP5 BAS16TW SOT-363
XW4 SM — +1_5V_AGP
XW9 SM

M10 Power Shut down Sequencing

+1_5V_GPU_VDD15 (500mA)

C448 0.01uF 20% 16V CERM 402
C443 0.01uF 20% 16V CERM 402
C435 0.01uF 20% 16V CERM 402
C482 0.01uF 20% 16V CERM 402
C411 10uF 20% 6.3V CERM 805
C505 0.01uF 20% 16V CERM 402
C532 0.01uF 20% 16V CERM 402
C529 0.01uF 20% 16V CERM 402
C526 0.01uF 20% 16V CERM 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

C484 10uF 20% 6.3V CERM 805
C485 10uF 20% 6.3V CERM 805
C440 0.22uF 20% 6.3V CERM 402
C441 0.22uF 20% 6.3V CERM 402
C445 0.22uF 20% 6.3V CERM 402
C446 0.22uF 20% 6.3V CERM 402
C449 0.22uF 20% 6.3V CERM 402
C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF 20% 6.3V CERM 402
C451 0.22uF 20% 6.3V CERM 402
C494 0.22uF 20% 6.3V CERM 402
C498 0.22uF 20% 6.3V CERM 402
C509 0.22uF 20% 6.3V CERM 402
C510 0.22uF 20% 6.3V CERM 402
C512 0.22uF 20% 6.3V CERM 402
C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF 20% 6.3V CERM 402
C525 0.22uF 20% 6.3V CERM 402
C528 0.22uF 20% 6.3V CERM 402
C531 0.22uF 20% 6.3V CERM 402
C533 0.22uF 20% 6.3V CERM 402
C477 0.22uF 20% 6.3V CERM 402
C486 0.22uF 20% 6.3V CERM 402
C495 0.22uF 20% 6.3V CERM 402

R384 10K 5% 1/16W MF 402 — (GPIO0) — ATI_AGP_FBSKEW<0>
R387 10K 5% 1/16W MF 402 — (GPIO1) — ATI_AGP_FBSKEW<1>
R386 10K 5% 1/16W MF 402 — NO STUFF — (GPIO2) — ATI_X1CLK_SKEW<0>
R382 10K 5% 1/16W MF 402 — NO STUFF — (GPIO3) — ATI_X1CLK_SKEW<1>
R383 10K 5% 1/16W MF 402 — NO STUFF — (GPIO4) — ATI_BUS_CFG<0>
R385 10K 5% 1/16W MF 402 — NO STUFF — (GPIO5) — ATI_BUS_CFG<1>
R381 10K 5% 1/16W MF 402 — NO STUFF — (GPIO6) — ATI_BUS_CFG<2>

R393 10K 5% 1/16W MF 402 — NO STUFF
R396 10K 5% 1/16W MF 402 — NO STUFF
R395 10K 5% 1/16W MF 402 — NO STUFF
R391 10K 5% 1/16W MF 402 — NO STUFF
R392 10K 5% 1/16W MF 402 — NO STUFF
R394 10K 5% 1/16W MF 402 — NO STUFF
R390 10K 5% 1/16W MF 402 — NO STUFF

CRITICAL
U47
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

	F12	VDD15
	L6	VDD15
	T6	VDD15
	AB6	VDD15
	F17	VDD15
	G25	VDD15
	R25	VDD15
	AB25	VDD15
	AJ3	VDDC
	AF25	VDDC
	AG4	VDDC
	AH4	VDDC
	AF5	VDDC
	F6	VDDC
	G6	VDDC
	H6	VDDC
	P6	VDDC
	AD26	VDDC
	V6	VDDC
	W6	VDDC
	AC6	VDDC
	AD6	VDDC
	AE6	VDDC
	F7	VDDC
	F10	VDDC
	AE10	VDDC
	F11	VDDC
	AE11	VDDC
	F13	VDDC
	F14	VDDC
	AE14	VDDC
	AF14	VDDC
	W26	VDDC
	AF15	VDDC
	AE17	VDDC
	AC25	VDDC
	AE18	VDDC
	F23	VDDC
	F24	VDDC
	AE24	VDDC
	F25	VDDC
	M25	VDDC
	N25	VDDC
	W25	VDDC
	V25	VDDC
	G7	VSS
	G8	VSS
	G9	VSS
	G10	VSS
	G11	VSS
	G12	VSS
	G13	VSS
	G14	VSS
	G15	VSS
	G16	VSS
	G17	VSS
	G18	VSS
	G19	VSS
	G20	VSS
	G21	VSS
	G22	VSS
	G23	VSS
	G24	VSS
	H7	VSS
	H8	VSS
	H23	VSS
	H24	VSS
	J7	VSS
	J24	VSS
	K7	VSS
	K24	VSS
	L7	VSS
	L24	VSS
	M7	VSS
	M24	VSS
	N7	VSS
	N24	VSS
	P7	VSS
	P24	VSS
	R7	VSS
	R24	VSS
	T7	VSS
	T24	VSS
	U7	VSS
	U24	VSS
	V7	VSS
	V24	VSS
	W7	VSS
	W24	VSS
	Y7	VSS
	Y24	VSS
	AA7	VSS
	AA24	VSS
	AB7	VSS
	AB24	VSS
	AC7	VSS
	AC8	VSS
	AC23	VSS
	AC24	VSS
	AD7	VSS
	AD8	VSS
	AD9	VSS
	AD10	VSS
	AD11	VSS
	AD12	VSS
	AD13	VSS
	AD14	VSS
	AD15	VSS
	AD16	VSS
	AD17	VSS
	AD18	VSS
	AD19	VSS
	AD20	VSS
	AD21	VSS
	AD22	VSS
	AD23	VSS

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS
+5V_MAIN
+3V_GPU

C706 4.7uF 20% 25V CERM 1206
C708 4.7uF 20% 25V CERM 1206

CRITICAL
Q48
SI7860DP
SO-8-PWRPK

L64
2.1uH-11A
SM

D29
SM
MBRS130LT3

CRITICAL
Q49
IRF7832
SO-8

C704 22uF 20% 10V CERM 1210
CRITICAL C707 330uF 20% 6.3V TANT CASE-D4
CRITICAL C705 330uF 20% 6.3V TANT CASE-D4
CRITICAL C711 330uF 20% 6.3V TANT CASE-D4

OMIT XW19 JUMPER OPEN — GPU_VCORE

R329 4.99K 1% 1/10W MF 402
R328 18.2K 1% 1/16W MF 402 — GPU_PWRMSR
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402 — GPU_PWRMSR — HIGH_VCORE
R786 100K 5% 1/16W MF 402 — HIGH_VCORE_DIV
C846 0.1uF 20% 16V CERM 402 — GPU_PWRMSR

GPU_VCORE_CNTL_RC
GPU_VCORE_CNTL
Q25 2N7002DW SOT-363
R549 10K 5% 1/16W MF 402 — GPU_PWRMSR — GPU_VCORE_CNTL_L
C712 0.1uF 20% 16V CERM 402 — NO STUFF

R558 10K 5% 1/16W MF 402 — GPU_VCORE_PWR_SEQ
R555 33K 5% 1/16W MF 402 — GPU_VCORE_SEQ_L
Q51 2N3904 SM — GPU_VCORE_SEQ
Q52 2N3904 SM
R559 100K 5% 1/16W MF 402 — +1_5V_AGP
R556 100K 5% 1/16W MF 402 — +5V_MAIN
DP7 BAS16TW SOT-363 — SLEEP_L_LS5
DP7 BAS16TW SOT-363 — DCDC_EN

R343 0 5% 1/16W MF 402
R352 63.4K 1% 1/16W MF 402 — NO STUFF
C466 4.7UF 20% 10V CERM 1206 — 1778_GND
R357 100K 5% 1/16W MF 402 — 1778_SHDN_L
R339 20K 1% 1/16W MF 402 — 1778_ITH_RC
C455 470pF 5% 25V CERM 402
C465 220pF 5% 25V CERM 402
R344 0 5% 1/16W MF 402 — NO STUFF
R353 0 5% 1/16W MF 402
C480 0.1uF 20% 10V CERM 402

U32
LTC1778
SSOP
EXT VIN (9) VCC (11) VCC (10)
RUN/SS (1) ITH (5) VRNG (3) FCB (4) PGOOD (6) SGND (13) PGND
ION (7) BOOST (16) TG (15) SW (14) BG (12) VFB (8)
CRITICAL

1778_VCC
1778_VIN
1778_ION
1778_BST
1778_TG
1778_BG
1778_VFB
1778_ITH
1778_VRNG
1778_FCB
GPU_CORE_OK
GPU_VCORE_SW
GPU_VCORE_SW_F
1778_BST_RC

D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603
C431 0.1uF 20% 25V CERM 603
C481 0.1uF 20% 25V CERM 603
C838 0.001uF 20% 50V CERM 402 — NO STUFF

OMIT XW6 SM

M10 CORE PWR/LVDS/TMDS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

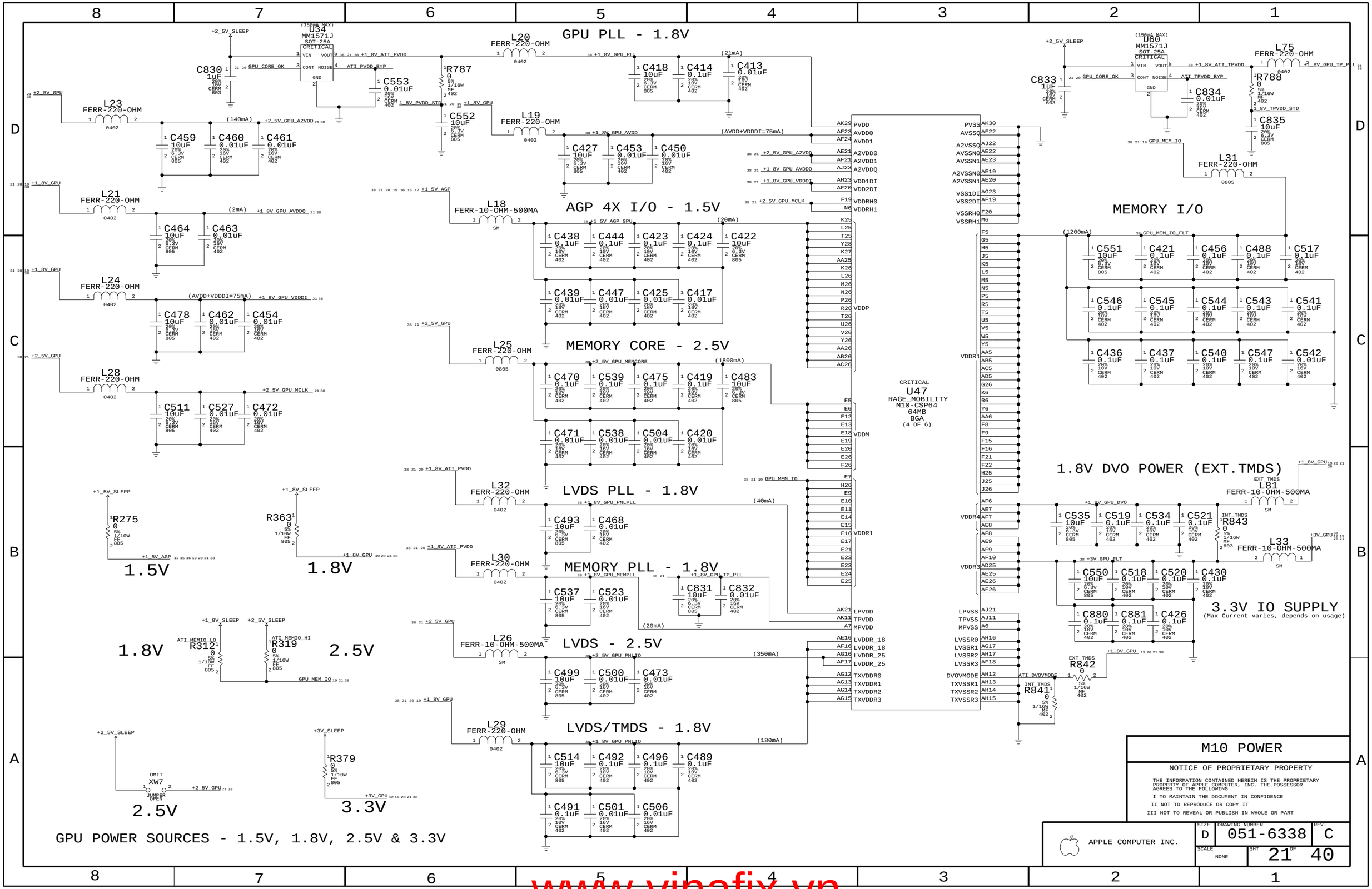
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 20 OF 40	

www.vinafix.vn



www.vinafix.vn

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN
U40 74AHC1G32 SM
L38 OMIT FERR-60-OHM-0.1A 0402
20 ATI_VSYNC → ATI_VSYNC_BUF → VGA_VSYNC 22 39
U39 74AHC1G32 SM
L36 OMIT FERR-60-OHM-0.1A 0402
20 ATI_HSYNC → ATI_HSYNC_BUF → VGA_HSYNC 22 39

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 90-OHM-300mA 2012H SYM_VER-1
39 37 19 TMDS_DN<0> → TMDS_CONN_DN<0>
39 37 19 TMDS_DP<0> → TMDS_CONN_DP<0>
L47 90-OHM-300mA 2012H SYM_VER-1
TMDS_DN<2> 39 19 37 → TMDS_CONN_DN<2>
TMDS_DP<2> 19 37 39 → TMDS_CONN_DP<2>
L46 90-OHM-300mA 2012H SYM_VER-1
TMDS_DN<1> 39 19 37 → TMDS_CONN_DN<1>
TMDS_DP<1> 39 19 37 → TMDS_CONN_DP<1>
L37 370-OHM SM SYM_VER-1
37 19 TMDS_CLKP → TMDS_CONN_CLKP 22 36 39
37 19 TMDS_CLKN → TMDS_CONN_CLKN 22 36 39

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L50 0.068uH SM
L49 0.068uH SM
L44 0.068uH SM
L43 0.068uH SM
L41 0.068uH SM
L40 0.068uH SM
20 GPU_B → GPU_B_FILTR → VGA_B 22 39
20 GPU_G → GPU_G_FILTR → VGA_G 22 39
20 GPU_R → GPU_R_FILTR → VGA_R 22 39
C642 4.7pF 5% 50V CERM 402
C641 3.3pF 0.25% 50V CERM 402
C635 4.7pF 5% 50V CERM 402
C634 3.3pF 0.25% 50V CERM 402
C632 4.7pF 5% 50V CERM 402
C631 3.3pF 0.25% 50V CERM 402
R462 75 1% 1/16W MF 402
R458 75 1% 1/16W MF 402
R456 75 1% 1/16W MF 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP
F2 CRITICAL 0.5AMP-13.2V SM
L42 400-OHM-EMI SM-1
+5V_DDC_SLEEP 22 38 39 → +5V_DDC_SLEEP_UF 38

Isolation required for DVI power switch

D19 SM MBR0530
DDC_CLK_ISO
R476 4.7K 5% 1/16W MF 402
R478 4.7K 5% 1/16W MF 402
R479 100 5% 1/16W MF 402
R477 100 5% 1/16W MF 402
R469 100 5% 1/16W MF 402
DVI_DDC_CLK
DVI_DDC_DATA
DVI_HPD
C654 100pF 5% 25V CERM 201
C655 100pF 5% 25V CERM 201
C653 100pF 5% 25V CERM 201
C667 0.01uF 20% 50V CERM 603
R464 0 5% 1/16W MF 402
PLACE NEAR C5A & C5B
R463 0 5% 1/16W MF 402
PLACE NEAR 3, 11 & 19
CHGND1
CHGND2

J22 CRITICAL QH1112 F-RT-TH
CHGND1
TMDS_CONN_DN<0>
TMDS_CONN_DP<0>
TMDS_CONN_DN<1>
TMDS_CONN_DP<1>
TMDS_CONN_DN<2>
TMDS_CONN_DP<2>
(TMDS_DN<5>) NC
(TMDS_DP<5>) NC
(TMDS_DN<4>)
(TMDS_DP<4>)
(TMDS_DN<3>)
(TMDS_DP<3>)
NC NC NC NC
39 22 DVI_DDC_CLK_UF
(+5V_DDC_SLEEP)
39 22 DVI_DDC_DATA_UF
39 22 DVI_HPD_UF
39 36 22 TMDS_CONN_CLKP
39 36 22 TMDS_CONN_CLKN
39 22 VGA_B → VGA_R 22 39
39 22 VGA_HSYNC → VGA_G 22 39
VGA_VSYNC 22 39
CHGND2

3V LEVEL SHIFTERS

+3V_SLEEP
Q39 2N7002DW SOT-363
Q39 2N7002DW SOT-363
Q40 2N7002DW SOT-363
R480 10K 5% 1/16W MF 402
R474 10K 5% 1/16W MF 402
R481 100K 5% 1/16W MF 402
DVI_DDC_CLK → GPU_DVI_DDC_CLK 20
DVI_DDC_DATA → GPU_DVI_DDC_DATA 20
DVI_HPD → GPU_HPD 20
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, +5V will be driven into DDC_CLK. Since host rails will be low, TP6610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP6610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q38 TP6610 SM
39 22 DVI_DDC_CLK_UF
39 38 +5V_DDC_SLEEP
R473 680 5% 1/16W MF 402
DVI_TURN_ON → DVI_TURN_ON_1LIM
R460 10K 5% 1/16W MF 402
R459 330 5% 1/16W MF 402
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.
Q35 MMDT3904 SOT-363
DVI_TURN_ON_BASE
SOFT_PWR_ON_L 23 29 33 39

+3V_SLEEP
Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.
R485 68.1K 1% 1/16W MF 402
C668 0.1uF 20% 10V CERM 402
U42 LMC7211 SM
R472 10K 1% 1/16W MF 402
DVI_HPD_UF → DVI_HPD_DIV
R484 100K 1% 1/16W MF 402
R482 10K 1% 1/16W MF 402
HPD_4V_REF
HPD_REF_EN_L
R475 10K 5% 1/16W MF 402
HPD_PWR_SW_BASE
HPD_PWR_SW
R470 330 5% 1/16W MF 402
Q35 MMDT3904 SOT-363
Q40 2N7002DW SOT-363
20 HPD_PWR_SNS_EN
R483 470K 5% 1/16W MF 402

INVERTER INTERFACE

+PBUS
L73 FERR-1K-OHM-EMI SM
+14V_INV
+5V_MAIN
Q76 FDG6324L SC70-6
+5V_INV_UF_SW 38
L74 400-OHM-EMI SM-1
R750 100K 5% 1/16W MF 402
FP_PWR_EN_L
C813 10uF 20% 6.3V CERM 805
+5V_INV_SW 39 38
Q76 FDG6324L SC70-6
22 20 FP_PWR_EN
C812 0.001uF 20% 50V CERM 402
C815 0.001uF 20% 50V CERM 402
J4 SM-2MT
L72 400-OHM-EMI SM-1
BRIGHT_PWM
INV_GND
+3V_MAIN
C22 0.1uF 20% 10V CERM 402
20 INV_ON_PWM
U2 NC7S32 SC70
BRIGHT_PWM_UF
C816 0.001uF 20% 50V CERM 402
C19 0.001uF 20% 50V CERM 402
L1 FERR-250-OHM SM
CHGND3

INVERTER EXPECTS ACTIVE HIGH SIGNAL

LCD INTERFACE

LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN
R347 100K 5% 1/16W MF 402
C474 2200pF 5% 50V CERM 603
R354 100K 5% 1/16W MF 402
LCD_PWREN_L
LCD_DIGON_L
Q28 2N7002 SM
22 20 FP_PWR_EN
TS3P SI3443DV Q29
+3V_LCD_SW 38
L27 FERR-250-OHM SM
+3V_LCD (LVDS DDC POWER) 39 38
C503 0.001uF 20% 50V CERM 402
+3V_SLEEP
R543 100K 5% 1/16W MF 402
R544 100K 5% 1/16W MF 402
C701 0.001uF 20% 50V CERM 402
LVDS_DDC_CLK 20 22 39
LVDS_DDC_DATA 20 22 39
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
NO STUFF
C702 0.001uF 20% 50V CERM 402
C548 0.001uF 20% 50V CERM 402
CHGND4
J14 CRITICAL G-501973 F-RT-SM

LVDS_DDC_CLK
LVDS_DDC_DATA
LVDS_L0N
LVDS_L0P
LVDS_L1N
LVDS_L1P
LVDS_L2N
LVDS_L2P
CLKLVDS_LN
CLKLVDS_LP
LVDS_U0N
LVDS_U0P
LVDS_U1N
LVDS_U1P
LVDS_U2N
LVDS_U2P
CLKLVDS_UN
CLKLVDS_UP
C549 0.001uF 20% 50V CERM 402
CHGND4

R753 0 5% 1/16W MF 402
C819 0.01uF 20% 50V CERM 603
CHGND3

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM
38 GPU_TV_GND1
L54 FERR-10-OHM-500MA SM
TV_GND1 38 39
20 GPU_Y
L53 3.3uH 0603
C657 0.01uF 20% 50V CERM 603
C663 560pF 10% 50V CERM 402
C656 560pF 10% 50V CERM 402
TV_C 39
20 GPU_C
L57 3.3uH 0603
C661 560pF 10% 50V CERM 402
C660 560pF 10% 50V CERM 402
TV_Y 39
20 GPU_COMP
L55 3.3uH 0603
C664 560pF 10% 50V CERM 402
C658 560pF 10% 50V CERM 402
TV_COMP 39
J21 CRITICAL MINIDIN RT-TH MH11773-WMR8A
CHGND1
XW14 SM
38 GPU_TV_GND2
L56 FERR-10-OHM-500MA SM
TV_GND2 38 39
C659 0.01uF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

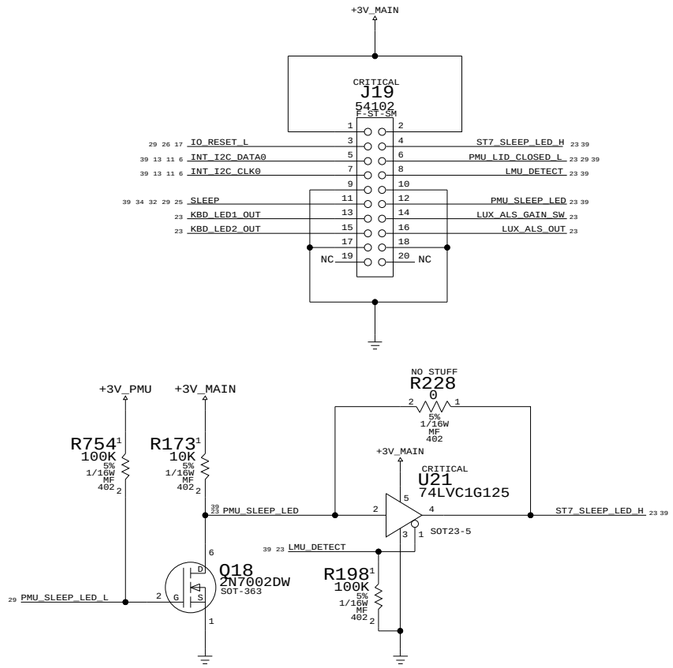
VIDEO CONNECTORS

APPLE COMPUTER INC.

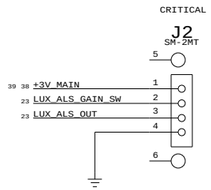
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 22 OF 40	

www.vinafix.vn

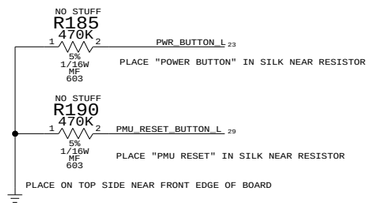
LMU/RIGHT SENSOR CONNECTOR



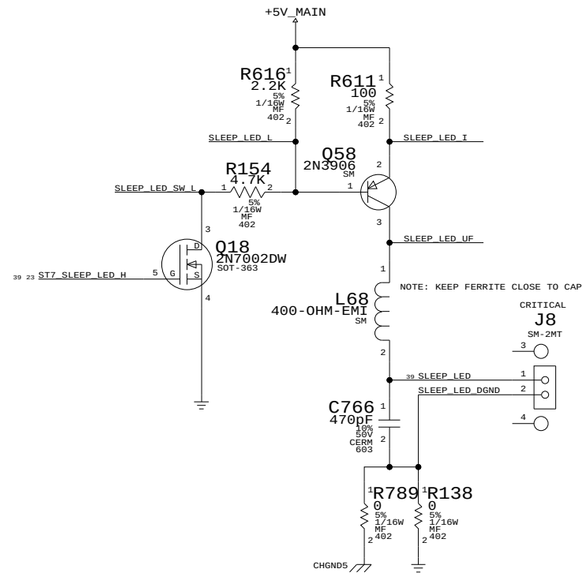
LEFT LIGHT SENSOR CONNECTOR



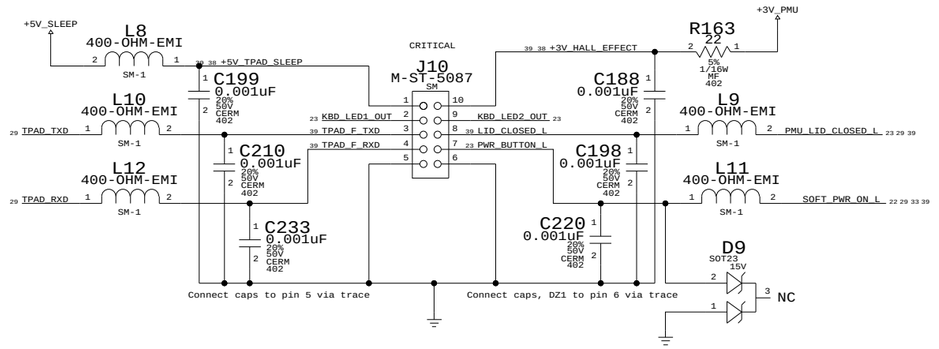
DEBUG HELPERS



SLEEP LED

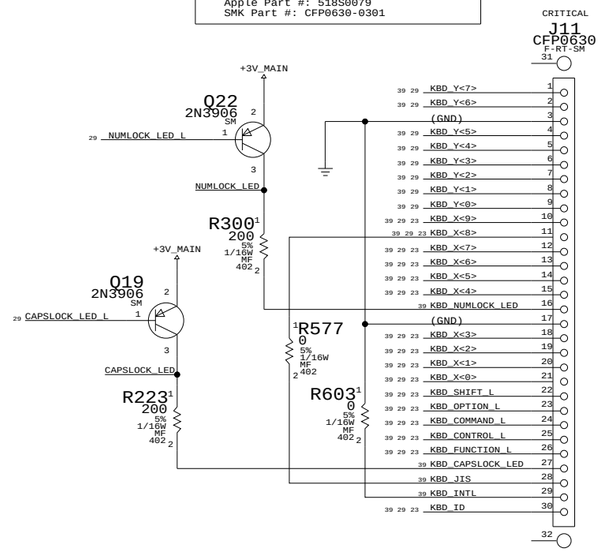


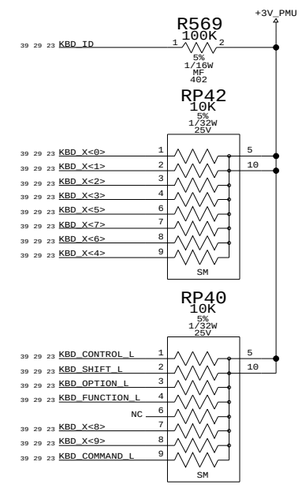
TRACKPAD/PWR BTN CONN



TOP CONTACT ZIF KEYBOARD CONN

CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301





KEYBOARD PULLUPS

KEYBOARD/TPAD/SLEEP LED

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C

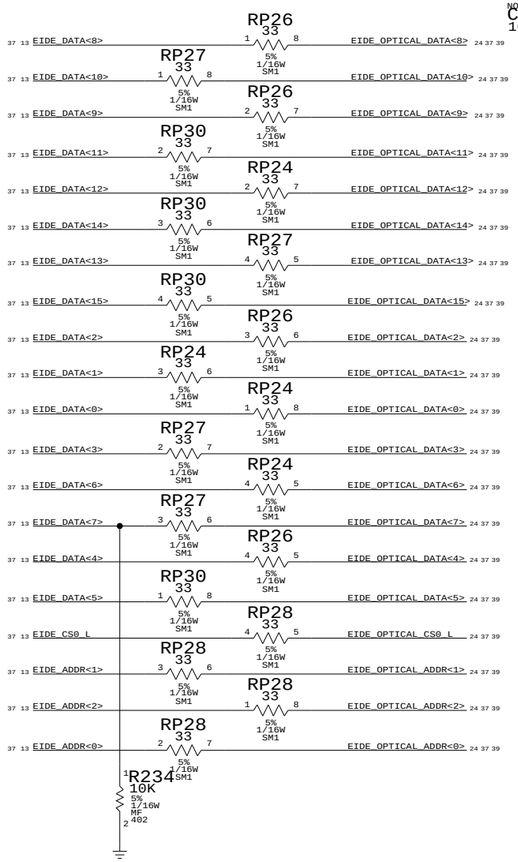
SCALE: NONE

SHT 23 OF 40

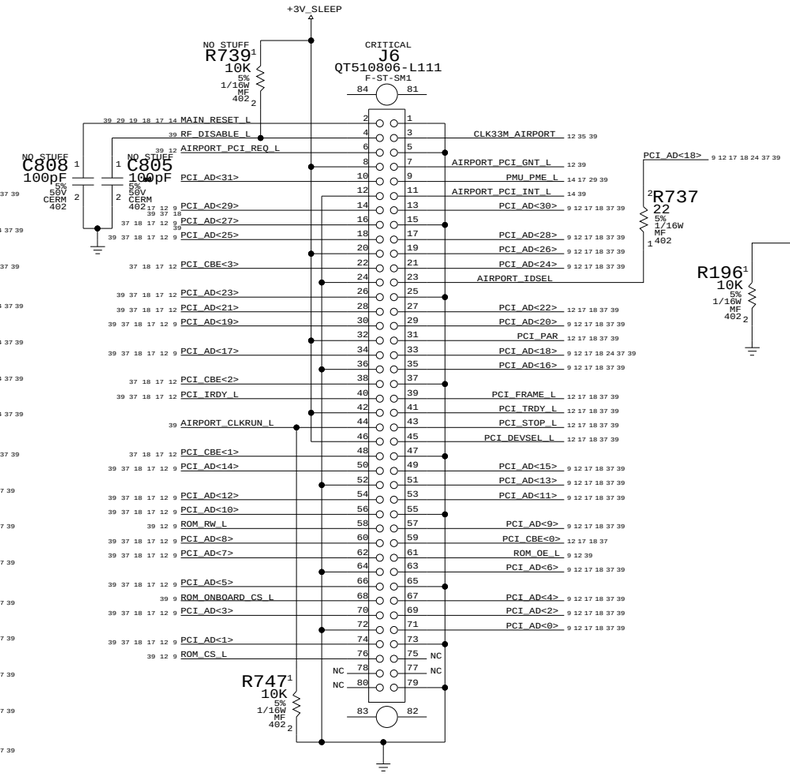
www.vinafix.vn

EIDE SERIES TERMINATION

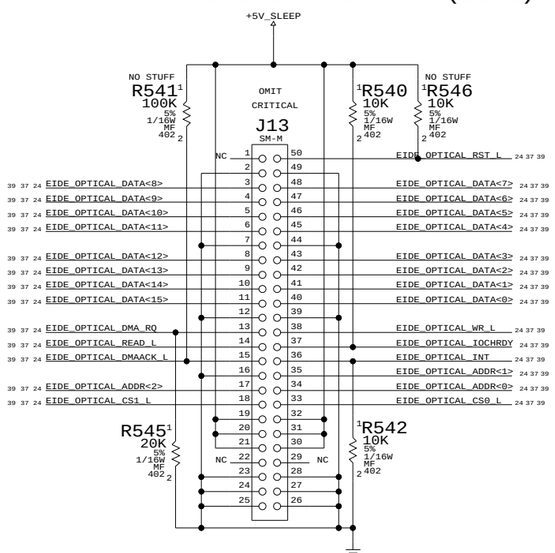
PLACE TERMINATORS NEAR INTREPID



WIRELESS INTERFACE

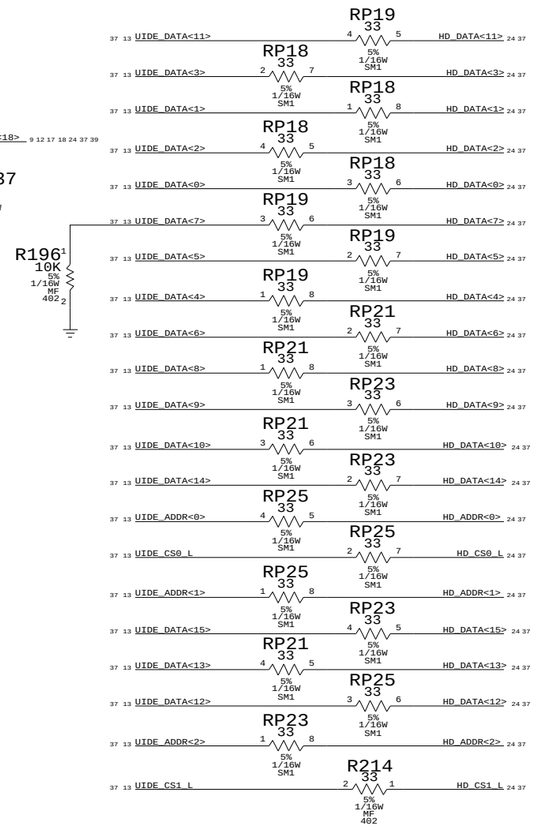


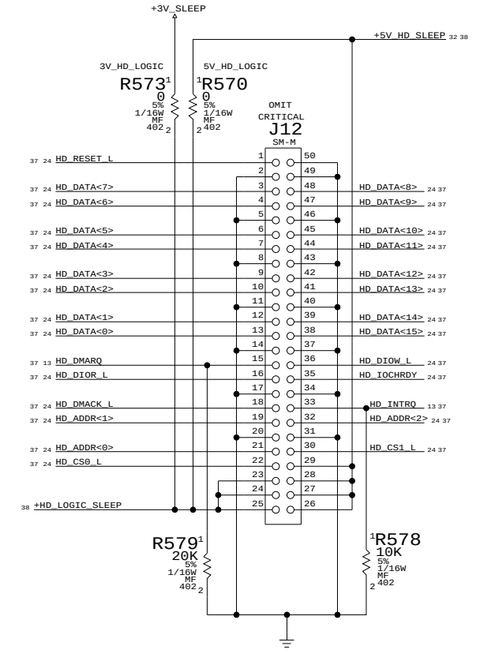
OPTICAL DRIVE INTERFACE (EIDE)



HARD DRIVE INTERFACE (UATA100)

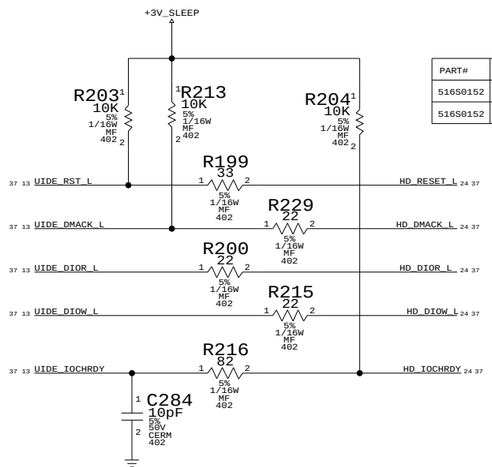
PLACE SERIES R CLOSE TO INTERPID





ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J12	CRITICAL	?
516S0152	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,50P,GOLD	J13	CRITICAL	?

INTERNAL I/O CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

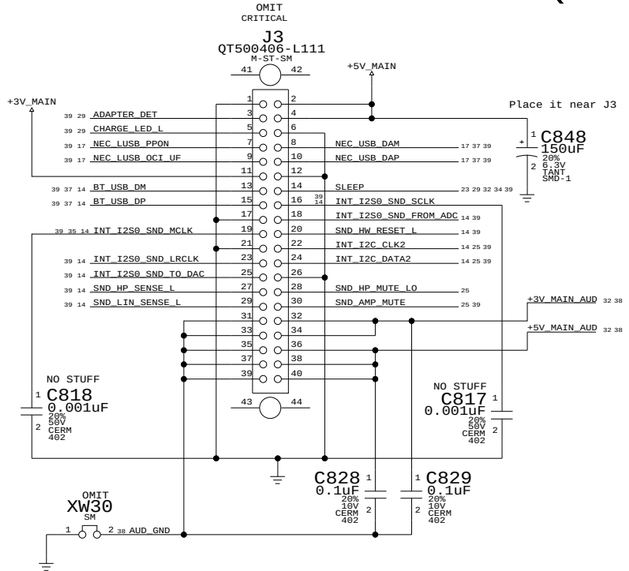
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

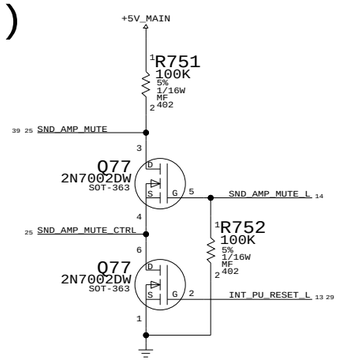
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 24 OF 40	

www.vinafix.vn

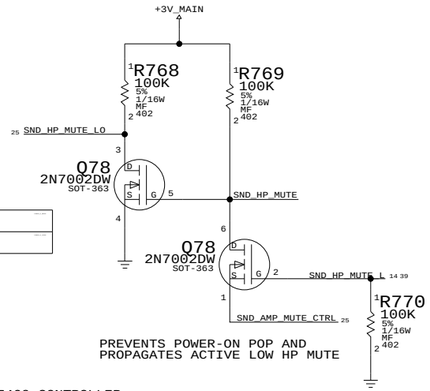
LEFT I/O & AUDIO BOARD (LIO)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0154	1	CONN,PLUG,0.5MM PITCH,1.5MM STACK,40P,GOLD	J3	CRITICAL	?

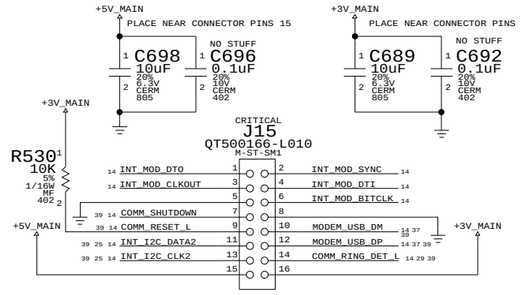


PREVENTS POWER-ON POP AND
GENERATES ACTIVE HIGH SPKR MUTE



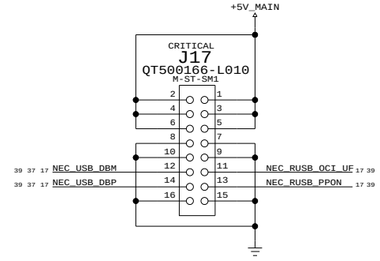
PREVENTS POWER-ON POP AND
PROPAGATES ACTIVE LOW HP MUTE

USB MODEM/SOFT MODEM

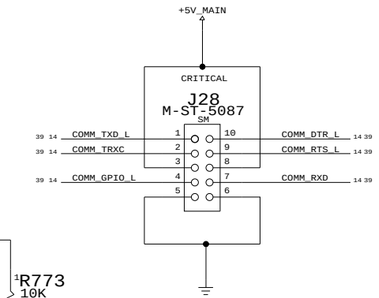


MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

RIGHT USB BOARD

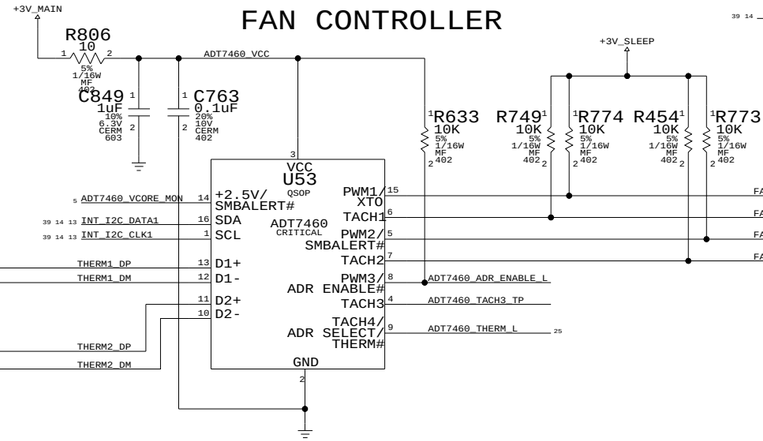


SERIAL DEBUG INTERFACE

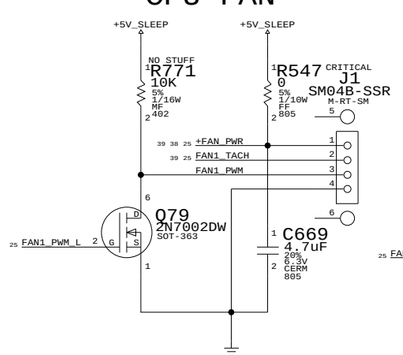


FAN INTERFACE

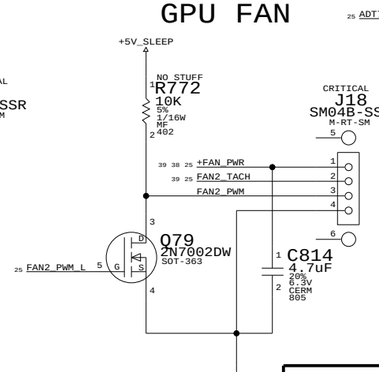
FAN CONTROLLER

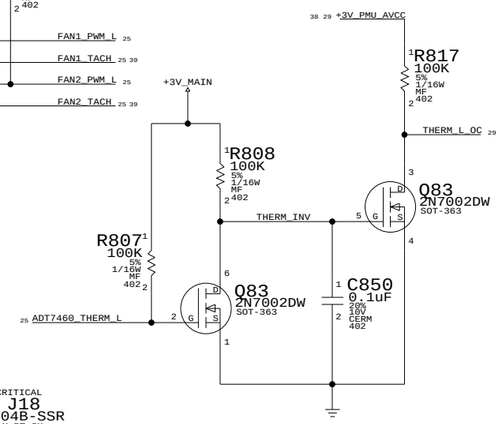


CPU FAN

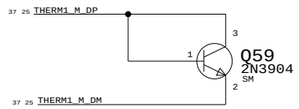


GPU FAN

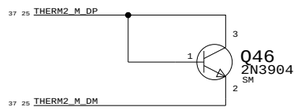




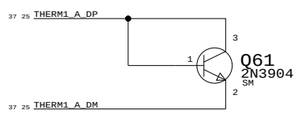
PLACE CLOSE TO CPU
MAIN1



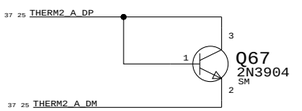
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



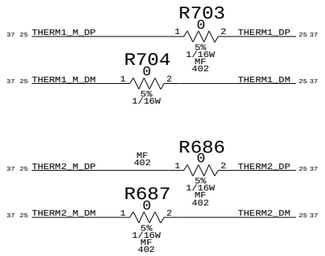
PLACE UNDERNEATH UPPER RAM
ALTERNATE1



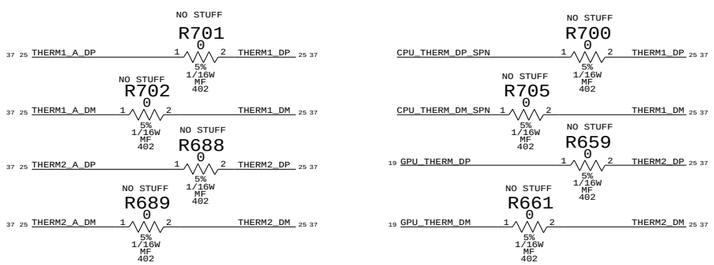
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



FAN/MODEM/SOUND/BACKUP BATT.

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 25 OF 40	

www.vinafix.vn

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/10W MF 402

3405_MODE

R507 0 5% 1/10W MF 402

U45 LTC3405 SOT23-6 CRITICAL
VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW 38

CRITICAL L60 3.3uH SM1

+1.0V_MARVELL 38

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

C674 10uF 20% 6.3V CERM 805

3405_VFB

R503 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — 35 13 CLKENET_LINK_TX — 35 CLKENET_PHY_TX

R421 0 5% 1/16W MF 402 — 35 13 CLKENET_LINK_RX — 35 CLKENET_PHY_RX

R445 0 5% 1/16W MF 402 — 35 13 CLKENET_LINK_GBE_REF — 35 CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402

C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

CRITICAL U43 88E1111 BCC

TX_CLK	4		
RX_CLK	2		
125CLK	22		
TXD0	11	37 13	ENET_PHY_TXD<0>
TXD1	12	37 13	ENET_PHY_TXD<1>
TXD2	14	37 13	ENET_PHY_TXD<2>
TXD3	16	37 13	ENET_PHY_TXD<3>
TXD4	17	37 13	ENET_PHY_TXD<4>
TXD5	18	37 13	ENET_PHY_TXD<5>
TXD6	19	37 13	ENET_PHY_TXD<6>
TXD7	20	37 13	ENET_PHY_TXD<7>
TX_EN	9	37 13	ENET_PHY_TX_EN
TX_ER	7	37 13	ENET_PHY_TX_ER
GTX_CLK	8	35 13	CLKENET_PHY_GTX
RXD0	95	37 13	ENET_LINK_RXD<0>
RXD1	92	37 13	ENET_LINK_RXD<1>
RXD2	93	37 13	ENET_LINK_RXD<2>
RXD3	91	37 13	ENET_LINK_RXD<3>
RXD4	90	37 13	ENET_LINK_RXD<4>
RXD5	89	37 13	ENET_LINK_RXD<5>
RXD6	87	37 13	ENET_LINK_RXD<6>
RXD7	86	37 13	ENET_LINK_RXD<7>
RX_DV	94	37 13	ENET_RX_DV
RX_ER	3	37 13	ENET_RX_ER
CRS	84	37 13	ENET_CRS
COL	83	37 13	ENET_COL
MDC	25	37 13	ENET_MDC
MDIO	24	37 13	ENET_MDIO
INT-/INT+	23	14	ENET_ENERGY_DET
RESET	28		ENET_RST_L
COMA	27		ENET_COMA
S_IN+	82	NC	
S_IN-	81	NC	
S_OUT+	77	NC	
S_OUT-	75	NC	
S_CLK+	79	NC	
S_CLK-	80	NC	
HSDAC+	37		ENET_HSDACP
HSDAC-	38		ENET_HSDACM
XTAL1	55		CLK25M_ENET_XIN
XTAL2	54		CLK25M_ENET_XOUT
VSSC	53		ENET_VSSC
CTRL10	51	NC	
DVDD	1, 6, 10, 15, 57, 62, 67, 71, 85		
VDDO	5, 21, 88, 96		
VDDOH	52, 66, 72		
VDDOX	26, 48		
AVDD	32, 35, 36, 40, 45, 78		
MDI0+	29	39 37	MDI_P<0>
MDI0-	31	39 37	MDI_M<0>
MDI1+	33	39 37	MDI_P<1>
MDI1-	34	39 37	MDI_M<1>
MDI2+	39	39 37	MDI_P<2>
MDI2-	41	39 37	MDI_M<2>
MDI3+	42	39 37	MDI_P<3>
MDI3-	43	39 37	MDI_M<3>
LED_LINK10	76		LED_LINK10
LED_LINK100	74		LED_LINK100
LED_LINK1000	73	NC	
LED_DUPLEX	70	NC	
LED_RX	69		LED_RX_SPN
LED_TX	68	NC	
CONFIG0	65	(000)	
CONFIG1	64	(000)	
CONFIG2	63	(111)	
CONFIG3	61	(110)	
CONFIG4	60	(111)	
CONFIG5	59	(101)	
CONFIG6	58	(000)	
TDI	44		JTAG_ENET_TDI 13
TDO	50		JTAG_ASIC_TDO_TP 39
TCK	49		JTAG_ASIC_TCK 13 39
TMS	46		JTAG_ASIC_TMS 13 39
TRST	47		JTAG_ASIC_TRST_L 13 39
RSET	30		ENET_RSET
SEL_OSC	56	NC	
SEL_2.5V	13		
GND	97		

SEE CONFIG TABLES (BELOW)

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C594 0.1uF 20% 10V CERM 402
C601 0.01uF 20% 10V CERM 402
C608 0.1uF 20% 10V CERM 402
C619 0.01uF 20% 10V CERM 402
C603 0.1uF 20% 10V CERM 402
C599 0.01uF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

38 26 +2_5V_MARVELL

C597 0.1uF 20% 10V CERM 402
C612 0.01uF 20% 10V CERM 402
C623 0.1uF 20% 10V CERM 402
C600 0.01uF 20% 10V CERM 402
C598 0.1uF 20% 10V CERM 402
C595 10uF 20% 6.3V CERM 805

+2_5V_MAIN

R442 0 5% 1/16W MF 603

C646 0.1uF 20% 10V CERM 402
C648 0.1uF 20% 10V CERM 402
C645 0.1uF 20% 10V CERM 402
C647 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

L35 FERR-EMI-600-OHM SM

38 +2_5V_MARVELL_AVDD

C614 0.1uF 20% 10V CERM 402
C616 0.01uF 20% 10V CERM 402
C618 0.1uF 20% 10V CERM 402
C602 0.01uF 20% 10V CERM 402
C592 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

R433 49.9 1% 1/16W MF 402 — MDI0_PD
R435 49.9 1% 1/16W MF 402 — MDI1_PD
R437 49.9 1% 1/16W MF 402 — MDI2_PD
R439 49.9 1% 1/16W MF 402 — MDI3_PD

R434 49.9 1% 1/16W MF 402
R436 49.9 1% 1/16W MF 402
R438 49.9 1% 1/16W MF 402
R440 49.9 1% 1/16W MF 402

C622 0.01uF 20% 10V CERM 402
C613 0.01uF 20% 10V CERM 402
C615 0.01uF 20% 10V CERM 402
C617 0.01uF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

CRITICAL J23 MJ-R0016 F-RT-TH

PRIMARY: 13, 11, 5 ENET_CTAP, 6 ENET_CTAP, 1 MDI_0+, 2 MDI_0-, 3 MDI_1+, 4 MDI_1-, 7 MDI_2+, 8 MDI_2-, 9 MDI_3+, 10 MDI_3-, 12, 14

RJ45 CHIP SIDE

CHGND1

1CT:1CT, 75 OHM

SECONDARY: J1, J2, J3, J4, J5, J6, J7, J8

RJ45 CABLE SIDE

SHIELD — 1000PF, 2000V

38 26 +2_5V_MARVELL

R431 10K 5% 1/16W MF 402
R430 10K 5% 1/16W MF 402
R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402 — 14 INT_ENET_RST_L

D15 1N914 SOT23 — 29 23 17 IO_RESET_L — ENET_RST_L

ENET_COMA

Q32 2N7002DW SOT-363 — 30 29 28 AC_IN

Q32 2N7002DW SOT-363 — 34 33 32 20 18 SLEEP_L_LS5

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

C611 2.2uF 20% 10V CERM 805

NO STUFF R425 20K 5% 1/16W MF 402

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M — CLK25M_XTAL_IN

C604 27pF 5% 50V CERM 402
C624 27pF 5% 50V CERM 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402
NO STUFF R429 49.9 1% 1/16W MF 402
R428 10K 5% 1/16W MF 402
R427 4.99K 1% 1/16W MF 402

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

NOTICE OF PROPRIETARY PROPERTY

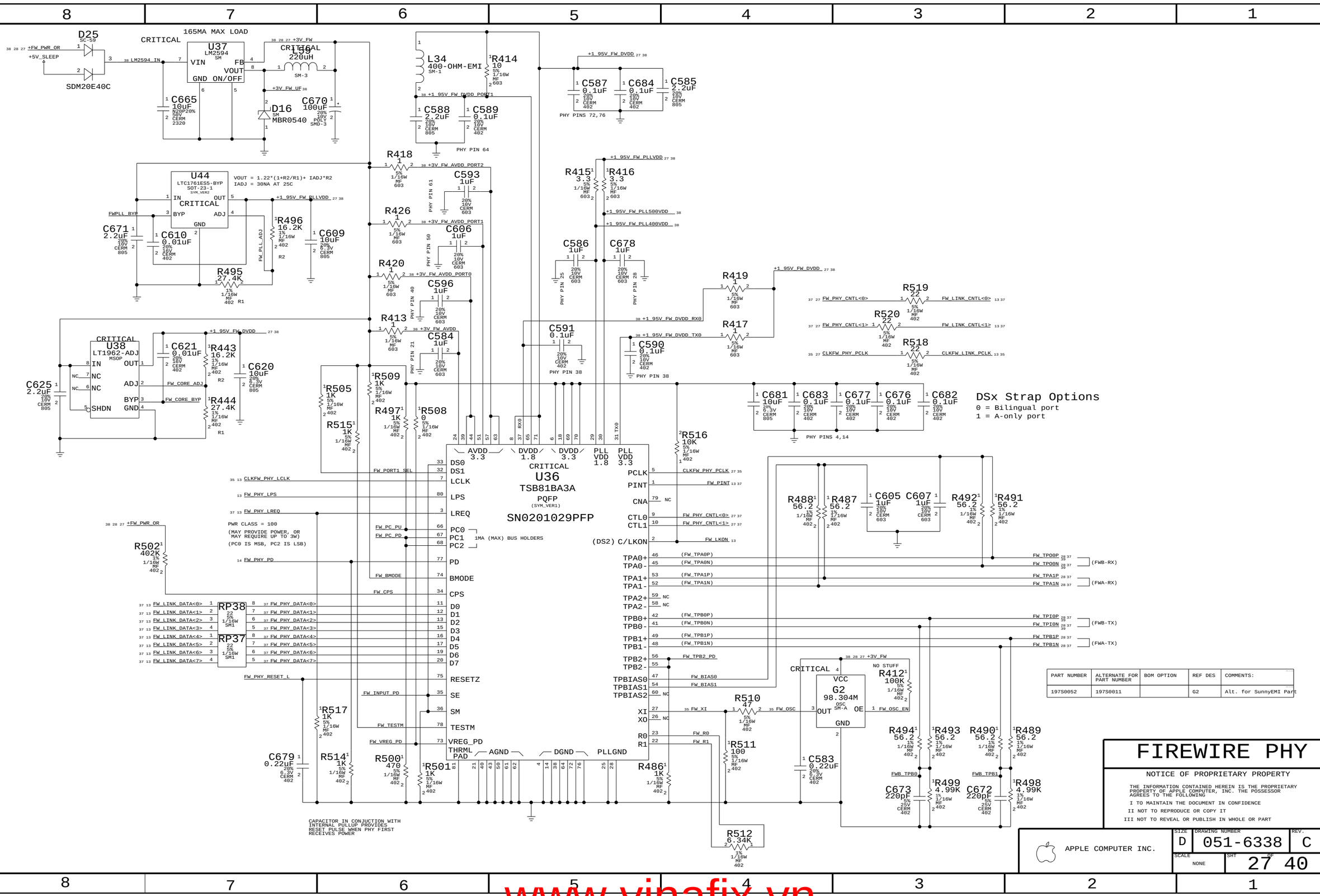
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

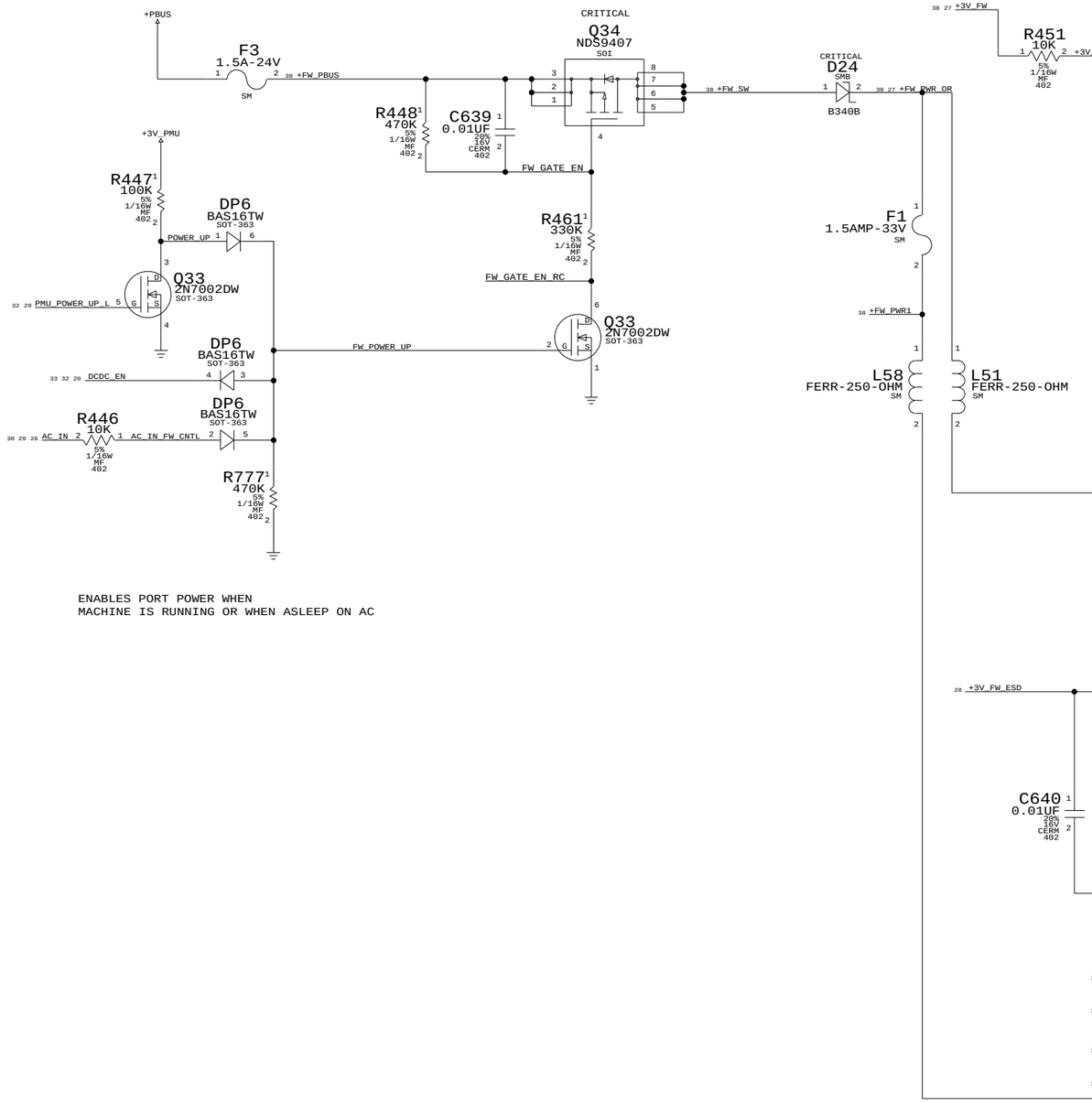
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 26 OF 40	

www.vinafix.vn



www.vinafix.vn

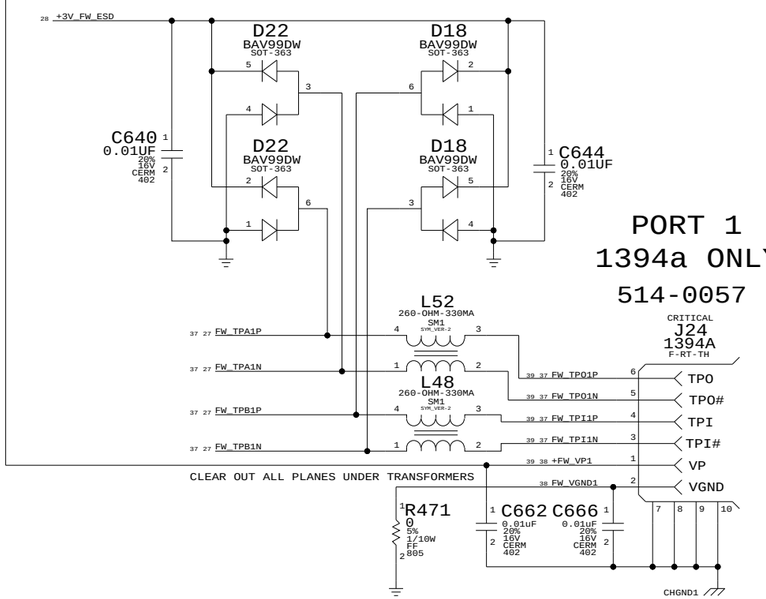
PORT POWER SWITCH



ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE,
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33



CLEAR OUT ALL PLANES UNDER TRANSFORMERS

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

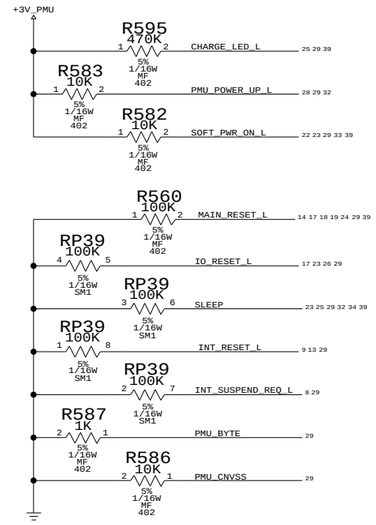
II NOT TO REPRODUCE OR COPY IT

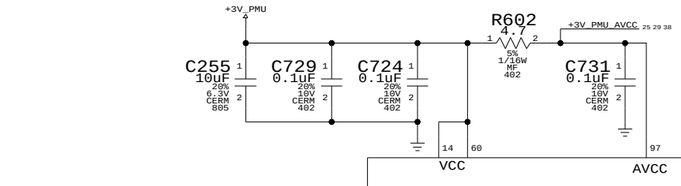
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

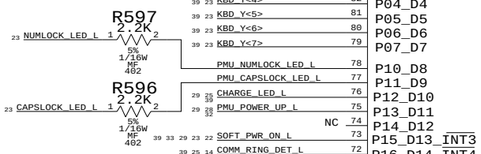
APPLE COMPUTER INC.

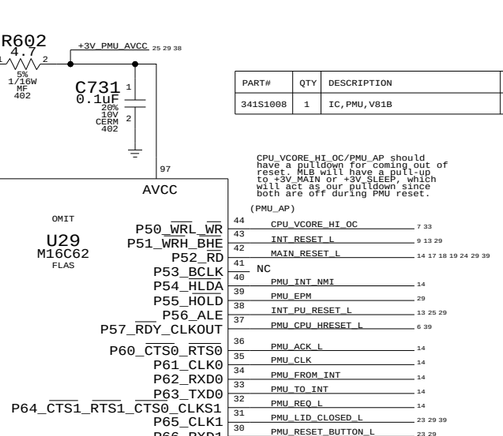
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 28 OF 40	

www.vinafix.vn





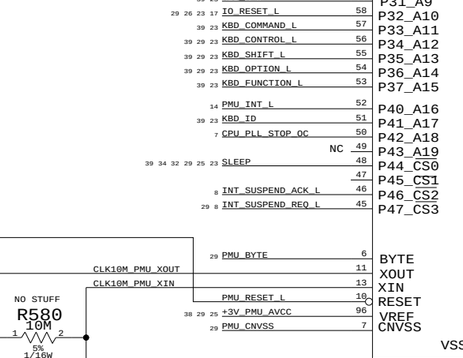




CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. HLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.

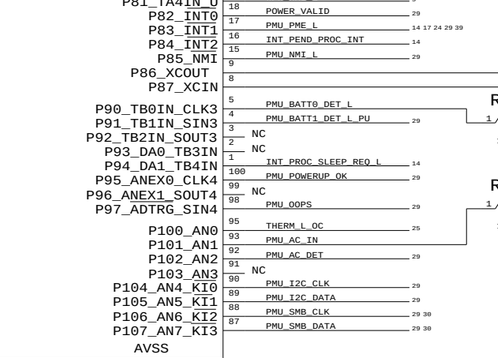
(PMU_AP)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U29	

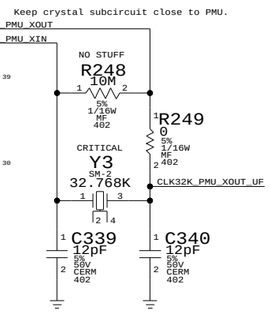


Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF

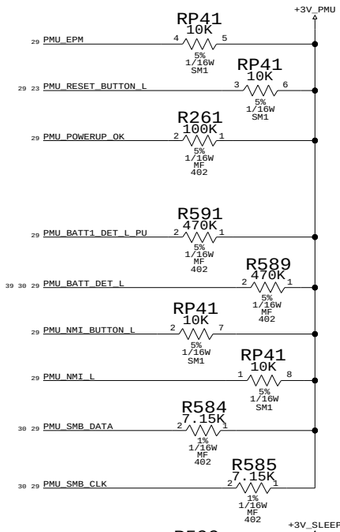
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0604	197S0041		Y4	Alt. for Siward Part

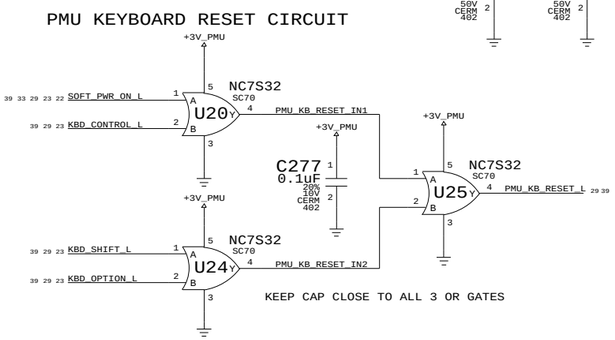


Keep crystal subcircuit close to PMU.

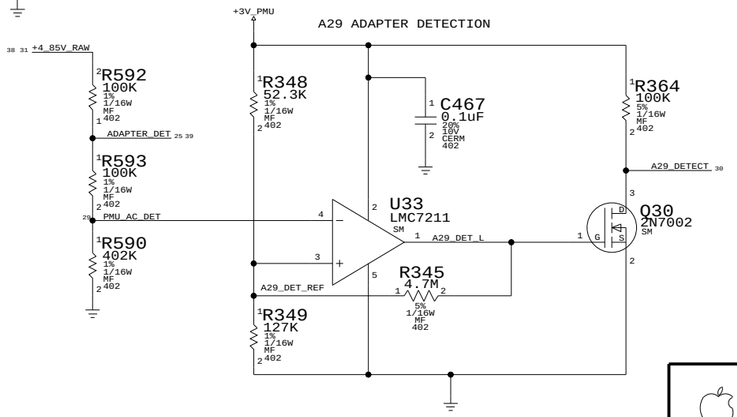


Y3'S LOAD CAPACITANCE IS 12.5PF





ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V



PMU

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 29 OF 40	

www.vinafix.vn

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 50V X7R 603

DC INRUSH LIMITER

Q68 SI4435DY SOI

R21 330K 5% 1/10W MF 402

C11 0.1uF 20% 50V CERM 805

GATE

AC_ENABLE_GATE

R51 20K 1% 1/16W MF 402

+3V_PMU

R40 97.6K 1% 1/16W MF 402

R16 100K 1% 1/10W MF 402

C801 0.01uF 20% 16V CERM 402

R15 10K 5% 1/16W MF 402

38 31 1V20_REF

U1 LMC7211 SM

AC_DIV

R42 10K 1% 1/16W MF 402

R30 57.6K 1% 1/16W MF 402

R41 1M 5% 1/16W MF 402

AC_IN 26 28 29 30

AC_IN_L 30

Q1 2N7002DW SOT-363

R29 470K 5% 1/16W MF 402

AC_ENABLE_L

Q1 2N7002DW SOT-363

R22 470K 5% 1/16W MF 402

GREATER THAN 13.1V DETECT

BACKFEED PROTECTION

Q69 SI4435DY SOI

38 +ADAPTER_SW

+ADAPTER_SENSE 38

BKFD_PROT_GATE

R732 47K 5% 1/16W MF 402

C803 0.1uF 20% 16V CERM 402

R734 68K 5% 1/16W MF 402

BKFD_PROT_EN_L

30 29 28 26 AC_IN

Q9 2N7002DW SOT-363

C36 0.01uF 20% 50V CERM 603

CRITICAL

U3 MAX4172 TSSOP

RS+ RS- PG OUT GND V+

NC NC NC NC

+24V_PBUS

MAX4172_OUT

CRITICAL

R77 2.21K 0.1% 1/16W MF 603

PLACE U24 NEXT TO R382

CRITICAL

R61 0.025 1% 1W MF 2512

R82 4.7 5% 1/4W MF 402

R87 4.7 5% 1/4W MF 402

1772_CSSP 37

1772_CSSN 37

CSSP CSSN

R57 100K 1% 1/16W MF 402

D4 1N914 SOT23

R49 12.7K 1% 1/16W MF 402

C67 1uF 20% 25V CERM 1210

C71 0.47uF 20% 50V CERM 1206

C95 0.47uF 20% 50V CERM 1206

38 1772_DCIN

30 1772_ACOK_L

(+3V_PMU)

1772_VCTL

1772_ICTL

1772_ICHG

1772_IINP

1772_CCV

1772_CCI

1772_CCS

DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS

U6 MAX1772 QSOP

CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT

1772_CELLS

1772_DLOV

1772_BST

1772_DHI

38 1772_LX

38 1772_DLO

(GND)

37 1772_CSIP

37 1772_CSIN

CRITICAL

C41 1uF 20% 16V CERM 603

REF CLS GND

1772_REF

1772_CLS

C43 0.01uF 20% 16V CERM 402

C42 0.01uF 20% 16V CERM 402

R55 1K 1% 1/16W MF 402

1772_CCV_RC

C24 0.1uF 10% 16V CERM 402

R83 1K 1% 1/16W MF 402

38 1772_GND

C23 1uF 20% 10V CERM 603

R54 10K 1% 1/16W MF 402

R53 4.12K 1% 1/16W MF 402

R56 1K 1% 1/16W MF 402

R94 100K 5% 1/16W MF 402

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402

IAC_RC_COMP

C798 0.1uF 20% 16V CERM 402

+3V_PMU

C794 0.1uF 20% 16V CERM 402

CRITICAL

R745 42.2K 0.1% 1/16W FF 603

IAC_FB

U55 LMC7111 SOT23-5

PLACE R383 CLOSE TO LTC1625

ROUTE LTC1625_ITH CAREFULLY

LTC1625_ITH

DP1 BAS16TW SOT-363

R119 150 1% 1/16W MF 402

1625_COMP 31

ADAPTER_I_REG

R727 10K 1% 1/16W MF 402

MAX4172_OUT

Place close to RS-

C826 0.01uF 20% 50V CERM 603

CURRENT_THRESHOLD

CRITICAL

R736 42.2K 0.1% 1/16W FF 603

CRITICAL

R738 82.5K 0.1% 1/16W FF 603

CRITICAL

R742 51.1K 0.1% 1/16W FF 603

A29_CURRENT_ADJ

Q2 2N7002DW SOT-363

30 29 A29_DETECT

R744 100K 5% 1/16W MF 402

AC_GTR_18V

OVER_18V_ADJ

Q74 2N7002DW SOT-363

Q74 2N7002DW SOT-363

30 1772_ACOK_L

C809 1uF 20% 16V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+BATT

+24V_PBUS

F5 5AMP-125V SM-2

+PBUS

F4 5AMP-125V SM-2

38 +BATT_24V_FUSE

38 +BATT_14V_FUSE

CRITICAL

Q6 SI4435DY SOI

CRITICAL

Q7 SUD45P03 TO-252

R716 47K 5% 1/10W MF 402

R710 47K 5% 1/10W MF 402

BATT_24V_GATE

BATT_14V_GATE

R717 10K 5% 1/16W MF 402

R711 10K 5% 1/16W MF 402

DP1 BAS16TW SOT-363

BATT_24PBUS_EN

BATT_14PBUS_EN

30 AC_IN_L

R102 158K 1% 1/16W MF 402

Q9 2N7002DW SOT-363

AC_IN_L_RC

C118 10uF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF

WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON

RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

+3V_PMU

R73 27.4K 1% 1/16W MF 402

R62 10K 1% 1/16W MF 402

R58 10K 1% 1/16W MF 402

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R74 4.12K 1% 1/16W MF 402

R733 20K 1% 1/16W MF 402

R731 1K 1% 1/16W MF 402

BATTV_HIGH

BATT_LOW_L

R59 100K 5% 1/16W MF 402

BATTV_LOW

Q4 2N7002DW SOT-363

R75 5.23K 1% 1/16W MF 402

Q71 2N7002DW SOT-363

Q71 2N7002DW SOT-363

29 PMU_CHARGE_V

Q4 2N7002DW SOT-363

+3V_PMU

R741 100K 5% 1/16W MF 402

Q72 2N7002DW SOT-363

CHARGE_DISABLE

Q72 2N7002DW SOT-363

29 PMU_CHRG_BATT_0

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

+3V_PMU

C799 0.1uF 20% 16V CERM 402

U57 LMC7211 SM

R729 100K 1% 1/16W MF 402

R740 499K 1% 1/16W MF 402

BATT_LOW

BATT_DIV

1V65_REF

R730 100K 1% 1/16W MF 402

R735 100K 1% 1/16W MF 402

C807 0.047uF 10% 16V CERM 402

30 29 A29_DETECT

Q2 2N7002DW SOT-363

R47 6.34K 1% 1/16W MF 402

A29_CLS_ADJ

38 +BATT_VSNS

BATTERY CONNECTOR

CRITICAL

J26 87438-0833 M-RT-SM

39 38 +BATT_POS

(BATT_IN_PD)

39 BATT_CLK

39 BATT_DATA

PMU_BATT_DET_L 29 39

39 38 BATT_NEG

L5 FERR-EMI-100-OHM SM

L2 FERR-50-OHM SM

L6 FERR-50-OHM SM

L4 FERR-EMI-100-OHM SM

PMU_SMB_CLK 29

L3 FERR-EMI-100-OHM SM

PMU_SMB_DATA 29

+BATT

1772_LDO 38

R725 33 5% 1/8W FF 1206

D6 1N914 SOT23

1772_BST_ESR

R52 100K 5% 1/16W MF 402

C97 0.1uF 20% 25V CERM 603

R96 4.7 5% 1/16W MF 603

+24V_PBUS

C96 0.1uF 20% 50V CERM 805

C112 2.2uF 20% 50V CERM 1812

C117 2.2uF 20% 50V CERM 1812

C113 2.2uF 20% 50V CERM 1812

C115 2.2uF 20% 50V CERM 1812

C116 2.2uF 20% 50V CERM 1812

CRITICAL

Q70 IRF7805 SM

CRITICAL

L70 10uH SM1

+BATT_RSNS 38

R715 0.05 1% 1W MF 2512

+BATT_24V_FUSE 30 38

D36 SM MBRS140T3

CRITICAL

Q64 IRF7811W SO-8

NO STUFF

C853 1000pF 10% 16V X7R 402

R720 1 1% 1/16W MF 603

R713 1 1% 1/16W MF 603

C780 4.7uF 20% 25V CERM 1206

C777 4.7uF 20% 25V CERM 1206

C795 4.7uF 20% 25V CERM 1206

C792 4.7uF 20% 25V CERM 1206

C790 4.7uF 20% 25V CERM 1206

C785 4.7uF 20% 25V CERM 1206

C779 33uF 20% 25V ELEC SM1

C98 0.1uF 20% 25V CERM 603

C99 0.1uF 20% 25V CERM 603

XW1 SM

R94 100K 5% 1/16W MF 402

BATTERY CHARGER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

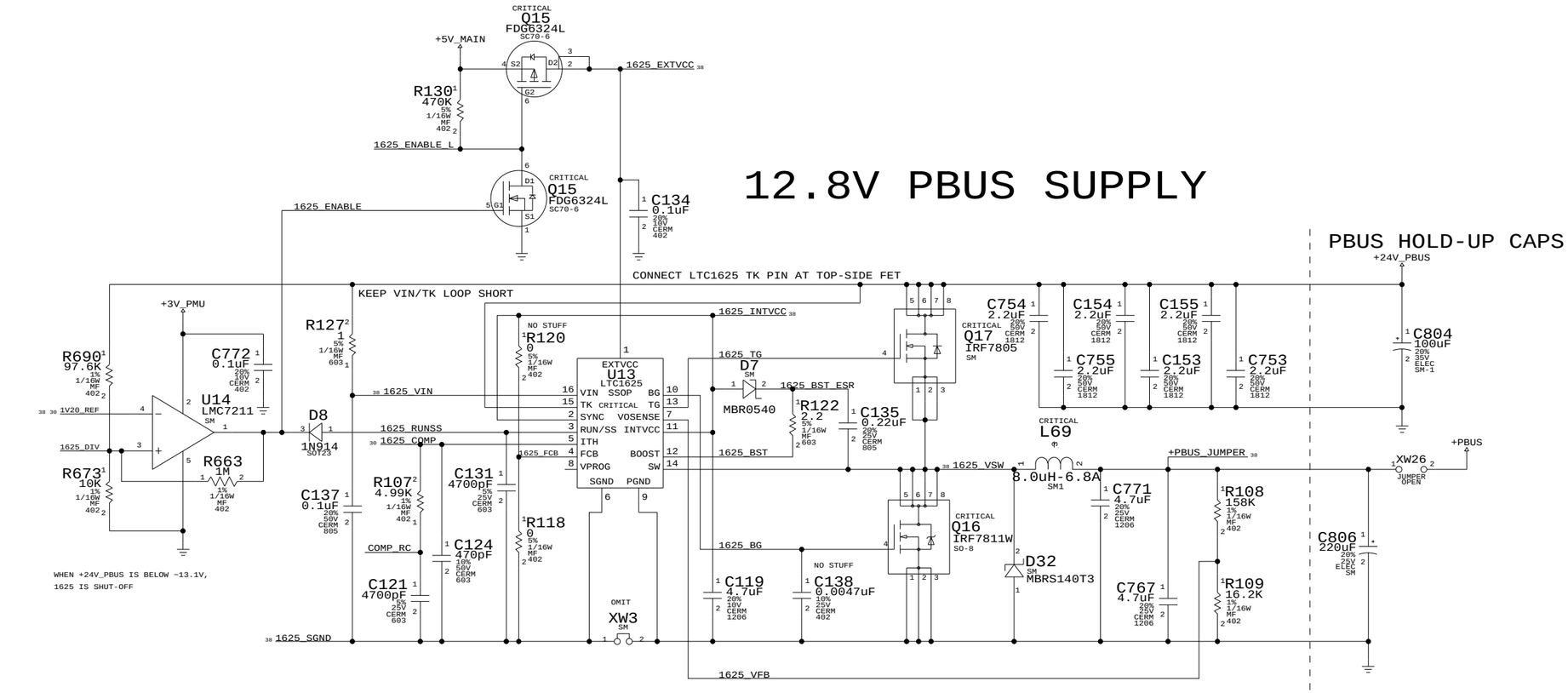
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

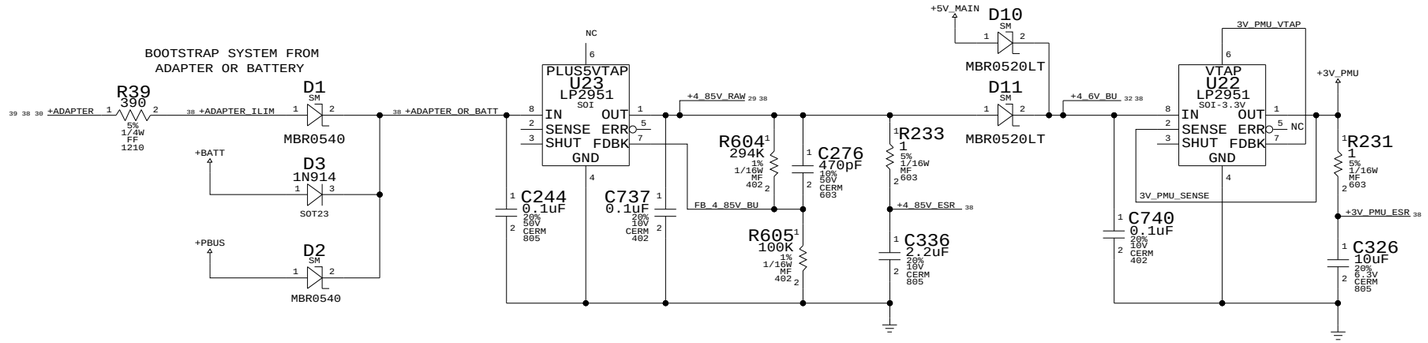
SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 30 OF 40	

www.vinafix.vn

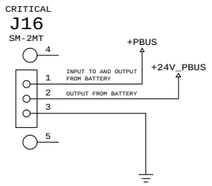
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

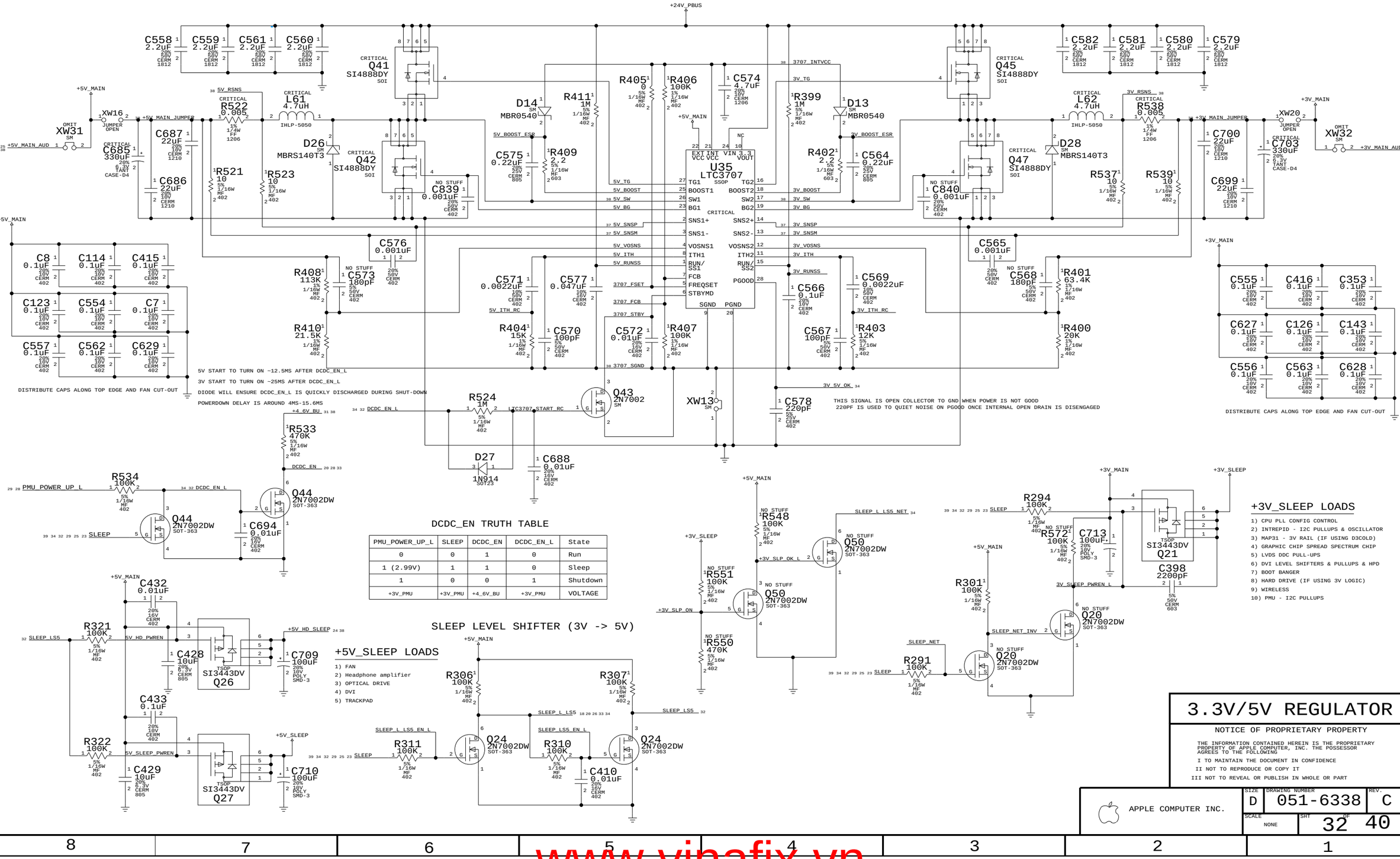
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 31 OF 40	

www.vinafix.vn

3.3V/5V MAIN SUPPLY



3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 32 OF 40	

www.vinafix.vn

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V->1.025V

1.300V->1.075V
1.225V->1.050V
(value without offset)

1.25Ghz
1.0Ghz

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

(For BEST config. R65 use 0-ohm RES,see BOM table)

Note:No stuff R67 to set skip mode of VCore

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

PLACE C423 CLOSE TO PINS 15 & 13!

Sense resistor R650 may not be needed!

Keep trace fat and short!!

(VCORE=1.385V for EVTB)

Connect MAX1717 GND pin 13 to GND at bottom-side FET

Keep trace fat and short!!

PLACE THIS SHORT AT PIN OF 1000uF CAP CLOSEST TO CPU

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.25Ghz 1.335V->1.080V
1.0Ghz 1.235V->1.060V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1000	1	RES,MF,0 ohm,5%,1/16W,0402,SMD	R65	?	CPU_BST
114S3573	1	RES,MF,1/16W,3.57K ohm,1%,0402,SMD	R97	?	CPU_BST

ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all
pull-downs are <=1K, $V_A = V_B$.

Fmax Test Connections

VCORE SUPPLY

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 33 OF 40	

www.vinafix.vn

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M10 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 34 OF 40	

www.vinafix.vn

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
				STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2				
GROUP 0	MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ
	MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ
	RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz
GROUP 2	MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ
	MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ
	RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz
	RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
DDR RAM	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	**(200)**			167.0 MHz
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	**(200)**	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	**(200)**			167 MHZ
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	**(200)**			167 MHZ
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	**(200)**			167.0 MHz
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	**(200)**			167 MHZ
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	**(200)**			167.0 MHz
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	**(200)**			167.0 MHz
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)			
	MEM_BA<1..0>	L:S::500	4					
	RAM_BA<1..0>	L:S:2000:3300	8		(200)			
CONTROL	MEM_CS_L<3..0>	L:S::500	4					
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)			
	MEM_CKE<3..0>	L:S::500	4					
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)			
	MEM_RAS_L	L:S::500 MIL	4					
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_CAS_L	L:S::500 MIL	4					
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)			
	MEM_WE_L	L:S::500 MIL	4					
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)			
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8					
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7					

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:3[illegible]	SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL			(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz
	INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz
	INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz
	CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING	
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING	
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING	
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING	
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING	
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING	
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING	
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING	
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV. C

SCALE NONE | SHT 35 OF 40

www.vinafix.vn

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)			
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)			
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)			
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)			
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)			
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)			
	CPU_TT<0..4>	L:S:1500:3400	7		(250)			
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)			

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

T231	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19	20
T233	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19	20
T232	GPU_TMDS_DN<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20
T234	GPU_TMDS_DP<0>	GPU_TMDS_D0	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20
T235	GPU_TMDS_DN<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20
T236	GPU_TMDS_DP<1>	GPU_TMDS_D1	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20
T238	GPU_TMDS_DN<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20
T237	GPU_TMDS_DP<2>	GPU_TMDS_D2	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19	20

T240	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	5	19	
T239	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	5	19	
T242	SI_TMDS_DN<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	
T241	SI_TMDS_DP<0>	SI_TMDS_D0	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	
T243	SI_TMDS_DN<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	
T245	SI_TMDS_DP<1>	SI_TMDS_D1	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	
T244	SI_TMDS_DN<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	
T246	SI_TMDS_DP<2>	SI_TMDS_D2	SITMDS:G:L:S:0 MIL:50 MIL	100 OHM SPACING	8	19	

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

T263	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610		19	20
T265	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19	20
T264	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19	20
T267	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19	20
T266	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::	19	20
T255	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700		19	
T256	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19	
T260	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19	
T261	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19	
T262	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::	19	

T268	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	39
T269	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	39
T271	TMDS_CONN_DN<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	
T270	TMDS_CONN_DP<0>	CONN_TMDS_D0	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	
T272	TMDS_CONN_DN<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	
T273	TMDS_CONN_DP<1>	CONN_TMDS_D1	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	
T274	TMDS_CONN_DN<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	
T275	TMDS_CONN_DP<2>	CONN_TMDS_D2	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	4	22	

SIGNAL CONSTRAINTS - PAGE 1

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C

SCALE: NONE | SHT 36 OF 40

www.vinafix.vn

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>	L:S:1650:1450	7					66 MHZ	12 19
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP BYTES 2-3	AGP_AD_STB_L<0>	L:S:1650 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ	12 19
	AGP_AD_STB_L<1>	L:S:1650 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ	12 19
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ	12 19
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ	12 19
	AGP_SB_STB_L	L:S:1650 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ	12 19
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHZ	12 19
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	9 12 17 18 24 39
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ	12 17 18 24
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ	12 17 18 24 39
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ	13 24
	UIDE_DATA<7>	U51_V1:RP19_3::600 MIL			(200)			100.0 MHZ	13 24
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ	13 24
	UIDE_ADDR<2..0>	L:S::650			(200)			100 MHZ	13 24
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ	13 24
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ	13
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ	13 24
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ	13
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ	24
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ	24
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ	24
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ	13 24
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ	24
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ	13 24
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ	13 24
	EIDE_ADDR<2..0>	L:S::850						33 MHZ	13 24
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ	13 24
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_INT	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ	13 24
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ	13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ	24 39
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ	24 39
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_RX_DV	L:S:8000 MIL:9000 MIL							13 26
	ENET_RX_ER	L:S:8000 MIL:9000 MIL							13 26
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)			13 26
	ENET_LINK_TXD<7..0>	L:S::600							13
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL							13 26
	ENET_LINK_TX_ER	L:S::400 MIL							13
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL							13 26
	ENET_LINK_TX_EN	L:S::400 MIL							13
	ENET_MDIO	L:S:8000 MIL:9000 MIL							13 26
	ENET_MDC	L:S:8000 MIL:9000 MIL							13 26
	ENET_COL	L:S:8000 MIL:9000 MIL							13 26
	ENET_CRS	L:S:8000 MIL:9000 MIL							13 26
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)			13 27
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)			27
	FW_LINK_CNTL<1..0>	L:S:9000:10000							13 27
	FW_PHY_CNTL<1..0>	L:S::300							27
	FW_LINK_LREQ	L:S::300 MIL							13
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL							13 27
	FW_PINT	L:S:8500 MIL:9500 MIL							13 27

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		27 28 39
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING		28
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		27 28
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING		28 39
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 10 MIL SPACING		26 39
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22 39
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	4	20 22
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING		20 22
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	5	19 22
	TMDS_DN<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<0>	TMDS_D0	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<1>	TMDS_D1	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DN<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	TMDS_DP<2>	TMDS_D2	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	19 22 39
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	5	20
	ATI_TMDS_DN<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<0>	ATI_TMDS_D0	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DP<1>	ATI_TMDS_D1	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING	8	20
	ATI_TMDS_DN<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
USB 1.1 Zo = 90	ATI_TMDS_DP<2>	ATI_TMDS_D2	ATITMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING	8	20
	USB_DEM	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DEP	USB_DE	USB_DE:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14
	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
USB 2.0 Zo = 90	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		10 MIL SPACING		14 25 39
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING		17 25 39
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL				30
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL				30
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL				32
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL				25
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL				25

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.6MIL (TRACE WIDTH)
S = 7MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV. C

SCALE NONE | SHT 37 OF 40

www.vinafix.vn

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	1394 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	1387 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1388 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	1389 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	1400 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 33 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	1555 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	1546 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1547 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	1548 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	1549 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1550 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	1551 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	1552 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	1553 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	1554 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	1555 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	1556 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	1561 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111 NEC USB2.0	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	1545 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	1547 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	1602 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	1611 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1645 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	1610 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1614 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	1606 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		31
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	1310 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14

SIGNAL CONSTRAINTS - PAGE 3

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6338	C
SCALE: NONE	SHT 38 OF 40	

www.vinafix.vn

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.

FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	JTAG_ASIC_TMS	TRUE			13 26
	JTAG_ASIC_TDI	TRUE			13
	JTAG_ASIC_TDO_TP	TRUE			26
	JTAG_ASIC_TCK	TRUE			13 26
	JTAG_ASIC_TRST_L	TRUE			13 26
	CPU_CHKSTP_OUT_L	TRUE			5
	CPU_SRESET_L	TRUE			5
	CPU_HRESET_L	TRUE			5 6 7
	JTAG_CPU_TMS	TRUE			5 6
	JTAG_CPU_TDI	TRUE			5 6
	JTAG_CPU_TDO_TP	TRUE			5
	JTAG_CPU_TCK	TRUE			5 6
	JTAG_CPU_TRST_L	TRUE			5 6
	INT_JTAG_TEI	TRUE			13
	INT_TST_MONIN_PD	TRUE			13
	INT_TST_MONOUT_TP	TRUE			13
	INT_TST_PLLEN_PD	TRUE			13
INT I2C	INT_I2C_CLK0	TRUE			6 11 13 23
	INT_I2C_DATA0	TRUE			6 11 13 23
	INT_I2C_CLK1	TRUE			13 14 25
	INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	+PBUS	TRUE			38
	+24V_PBUS	TRUE			38
	GPU_VCORE	TRUE			19 20 38
	1778_VFB	TRUE			20 38
	CPU_VCORE_SLEEP	TRUE			5 33 38
	VCORE_FB	TRUE			33 38
	+1_8V_MAIN	TRUE			38
	+2_5V_MAIN	TRUE			38
	+5V_MAIN	TRUE	2		38 39
	+5V_SLEEP	TRUE	2		38 39
	+3V_MAIN	TRUE	4		23 38
		TRUE		1000	IN
	+3V_PMU	TRUE			38
CARDBUS	CBUS_DET_1_L	TRUE		2000	18
	CBUS_DET_2_L	TRUE		2000	18
DVI	TMDS_DN<0..2>	TRUE		1000	19 22 37
	TMDS_DP<0..2>	TRUE		1000	19 22 37
	TMDS_CONN_CLKN	TRUE		1000	22 36
	TMDS_CONN_CLKP	TRUE		1000	22 36
	VGA_R	TRUE		1000	22
	VGA_G	TRUE		1000	22
	VGA_B	TRUE		1000	22
	VGA_HSYNC	TRUE		1000	22
	VGA_VSYNC	TRUE		1000	22
	DVI_DDC_CLK_UF	TRUE		1000	22
	DVI_DDC_DATA_UF	TRUE		1000	22
	DVI_HPD_UF	TRUE		1000	22
	+5V_DDC_SLEEP	TRUE		2000	22 38
CHGND1		TRUE	2	2000	IN
LVDS		TRUE	6	1000	IN
	LVDS_L0N	TRUE		1000	20 22 37
	LVDS_L0P	TRUE		1000	20 22 37
	LVDS_L1N	TRUE		1000	20 22 37
	LVDS_L1P	TRUE		1000	20 22 37
	LVDS_L2N	TRUE		1000	20 22 37
	LVDS_L2P	TRUE		1000	20 22 37
	CLKLVDS_LN	TRUE		1000	20 22 37
	CLKLVDS_LP	TRUE		1000	20 22 37
	LVDS_DDC_CLK	TRUE		1000	20 22
	LVDS_DDC_DATA	TRUE		1000	20 22
	+3V_LCD	TRUE	2	2000	22 38
	+3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	+14V_INV	TRUE		2000	22 38
	+5V_INV_SW	TRUE		2000	22 38
	BRIGHT_PWM	TRUE		2000	22
	INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	TV_C	TRUE		2000	22
	TV_Y	TRUE		2000	22
	TV_COMP	TRUE		2000	22
	TV_GND1	TRUE		2000	22 38
	TV_GND2	TRUE		2000	22 38
LIO	INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	INT_I2S0_SND_SCLK	TRUE		1000	14 25
	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	SND_HP_MUTE_L	TRUE		1000	14 25
	SND_AMP_MUTE	TRUE		1000	25
	SND_HW_RESET_L	TRUE		1000	14 25
	SND_HP_SENSE_L	TRUE		1000	14 25
	SND_LIN_SENSE_L	TRUE		1000	14 25
	INT_I2C_CLK2	TRUE		1000	14 25
	INT_I2C_DATA2	TRUE		1000	14 25
	ADAPTER_DET	TRUE		1000	25 29
	CHARGE_LED_L	TRUE		1000	25 29
	NEC_LUSB_OCI_UF	TRUE		1000	17 25
	NEC_LUSB_PPON	TRUE		1000	17 25
	+5V_MAIN	TRUE	2	2000	38 39
	+5V_SLEEP	TRUE	2	3000	38 39
	+3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	NEC_USB_DAM	TRUE			17 25 37
	NEC_USB_DAP	TRUE			17 25 37
	NEC_USB_DBM	TRUE			17 25 37
	NEC_USB_DBP	TRUE			17 25 37
	BT_USB_DM	TRUE			14 25 37
	BT_USB_DP	TRUE			14 25 37
	MODEM_USB_DM	TRUE			14 25 37
	MODEM_USB_DP	TRUE			14 25 37
RT. USB	NEC_RUSB_PPON	TRUE			17 25
	NEC_RUSB_OCI_UF	TRUE			17 25
WIRELESS	PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	PCI_STOP_L	TRUE		1000	12 17 18 24 37
	PCI_PAR	TRUE		1000	12 17 18 24 37
	AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	AIRPORT_PCI_INT_L	TRUE		1000	14 24
	MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	CLK33M_AIRPORT	TRUE		1000	12 24 35
	PMU_PME_L	TRUE		1000	14 17 24 29
	ROM_ONBOARD_CS_L	TRUE		1000	9 24
	ROM_OE_L	TRUE		1000	9 12 24
	ROM_CS_L	TRUE		1000	9 12 24
	ROM_RW_L	TRUE		1000	9 12 24
	RF_DISABLE_L	TRUE		1000	24
	AIRPORT_CLKRUN_L	TRUE		1000	24
	+3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	+5V_TPAD_SLEEP	TRUE		3000	23 38
	TPAD_F_TXD	TRUE		3000	23
	TPAD_F_RXD	TRUE		3000	23
	LID_CLOSED_L	TRUE		3000	23
	+3V_HALL_EFFECT	TRUE		3000	23 38
MODEM/ SERIAL	SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
	COMM_RESET_L	TRUE		4000	14 25
	COMM_SHUTDOWN	TRUE		4000	14 25
	COMM_RING_DET_L	TRUE		4000	14 25 29
	COMM_TXD_L	TRUE		4000	14 25
	COMM_TRXC	TRUE		4000	14 25
	COMM_GPIO_L	TRUE		4000	14 25
	COMM_DTR_L	TRUE		4000	14 25
	COMM_RTS_L	TRUE		4000	14 25
	COMM_RXD	TRUE		4000	14 25
KEYBOARD	KBD_ID	TRUE		3000	23 29
	KBD_INTL	TRUE		3000	23
	KBD_JIS	TRUE		3000	23
	KBD_CAPSLOCK_LED	TRUE		3000	23
	KBD_NUMLOCK_LED	TRUE		3000	23
	KBD_FUNCTION_L	TRUE		3000	23 29
	KBD_COMMAND_L	TRUE		3000	23 29
	KBD_OPTION_L	TRUE		3000	23 29
	KBD_CONTROL_L	TRUE		3000	23 29
	KBD_SHIFT_L	TRUE		3000	23 29
	KBD_X<0..9>	TRUE		3000	23 29
	KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_CLK	TRUE		1000	30
	BATT_DATA	TRUE		1000	30
	PMU_BATT_DET_L	TRUE		1000	29 30
FANS	+FAN_PWR	TRUE		3000	25 38
	FAN1_TACH	TRUE		3000	25
	FAN2_TACH	TRUE		3000	25
	FAN1_GND	TRUE		3000	38
	FAN2_GND	TRUE		3000	38
ETHERNET	MDI_P<0..3>	TRUE		1000	26 37
	MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	FW_TPO0P	TRUE		1000	27 28 37
	FW_TPO0N	TRUE		1000	27 28 37
	FW_TPO0R	TRUE		1000	28
	FW_TPI0P	TRUE		1000	27 28 37
	FW_TPI0N	TRUE		1000	27 28 37
	+FW_VP0	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	FW_TPO1P	TRUE		1000	28 37
	FW_TPO1N	TRUE		1000	28 37
	FW_TPI1P	TRUE		1000	28 37
	FW_TPI1N	TRUE		1000	28 37
	+FW_VP1	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	ST7_SLEEP_LED_H	TRUE			23
	PMU_SLEEP_LED	TRUE			23
	PMU_LID_CLOSED_L	TRUE			23 29
	LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
MISC.			(100 MIL PROBE PREFERRED)		
	SLEEP_LED	TRUE			23
	PMU_KB_RESET_L	TRUE			29
	SLEEP	TRUE			23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE			6 29
	BB_RESET_L	TRUE			6
	+3V_PMU_RESET	TRUE			29 33

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV. C

SCALE NONE | SHT 39 OF 40

www.vinafix.vn

REVISION HISTORY

Proto Release

7/22/02 - Initial acquisition of schematic (from 051-6278 Rev 01)
Added P59 SO-DIMM connector as placeholder (p.12)
Added P59 LVDS connector as placeholder (p.22)
Changed J9 to 10 pin Elco connector for modem (p.25)
Changed PBUS holdup caps to P59 electrolytic cans (p.30)
7/23/02 - Removed L3 (p.8)
Replaced processor with 360 pin Apollo (p.5,6)
7/24/02 - Added FETs between battery and PBUS rails for airline power (p.29)
8/10/02 - Added USB 2.0 (p.18)
8/20/02 - Removed spare pullup straps for Intrepid (p.9)
Removed USB overcurrent protection [to be placed on other boards] (p.18)
Changed right USB board connector to 16 pin Hirose connector (p.26)
Changed LIO board connector to 40 pin Molex connector (p.26)
Added 6 bypass caps to MAXBUS_SLEEP and CPU_VCORE_SLEEP (p.5)
8/26/02 - Removed 32 bypass caps for +3V_MAIN at Intrepid (p.16)
Removed 5 bypass caps for +2.5V_MAIN at Intrepid (p.16)
Removed 3 bypass caps for +1.5V_AGP at Intrepid (p.16)
Removed 4 bypass caps for MAXBUS_MAIN at Intrepid (p.16)
8/27/02 - Changed main battery connector to BP24067-R1, which is close to final (p.29)
8/29/02 - Added dedicated Boot Banger circuit (p.6)
Added 5 bypass caps to each SO-DIMM connector (p.11)
Added quad voltage circuit for bus slewing architecture (p.32)
8/30/02 - Changed to low profile 32.768kHz crystal for PMU (p.28)
Changed to Q11 adpater detection scheme (p.28)
9/03/02 - Corrected upper LVDS single pin nets (p.20)
Removed unintentional extra pulldown resistor at Intrepid (p.14)
9/17/02 - Numerous changes to stay in sync with P84 (all)
9/18/02 - Changed battery connector back to P84 part (p.29)
Added LMU circuitry to eliminate extra board (p.23)
Changed to P84 dual channel LVDS connector to reduce I2R cable losses(p.22)
9/19/02 - Removed unnecessary battery FETs [due to 3S only design] (p.29)
Modified chassis gnds on some components (all)
Removed LMU connector (p.23)
Corrected battery connector [same as P84] (p.29)
Removed P93 support (p.25)
Removed second fuse from FW ports [single fuse provides adequate power] (p.27)
9/23/02 - Replaced BCM5421 with Marvell 88E1111 (p.26)
Increased MAX_VIA_COUNT by two on most nets with this constraint for uVia (p.34,35)
9/27/02 - Corrected cpu, memory bus constraints to match manhattan lengths (p.34)
Swapped pins on L33, L35 for layout (p.31)
Changed Y6 to smaller form-factor crystal (p.26)
9/30/02 - Changed J19 (DC-in) to proper 4-pin connector (p.29)
Corrected holes and chassis gnds (p.4,all)
10/01/02 - Removed Intrepid 1.x specific circuitry (p.13)
10/03/02 - Numerous pin-swaps to accomodate board layout (all)
10/08/02 - Added page for functional test points (p.37)
10/09/02 - Changed 16 pin connectors (modem and right USB) to Foxconn parts (p.23)
10/10/02 - Clamped NEC NC pins high per documentation (p.17)
Added 10K pullup to CG_ADDRSEL and 10K pulldown to CG_FSEL on CY28512 (p.14)
Added RSCG/NO_SSCG stuffing options for CY28512 circuit (p.14)
Removed CPU_VGATE pullup to 5V to eliminate potential 3V/5V current path (p.32)
Removed Zebra 15/18 support per P84 (p.27)
Added second FW port power fuse (p.27)
Removed INT_CPUFB_IN cap per P84 (p.8)
Replaced IRF7822 FETs with IRF7811W in battery charger and 14V PBUS switchers (p.29,30)
Renamed optical interface for consistency (p.24,37)
Corrected PLL_CFG<4> for Apollo 7 (needs to always be zero) (p.5,7)
Removed temporary P84 constraints and finished up AGP clock changes (p.12,34)
Added stuffing options to power fans off 3V or 5V (p.25)
10/11/02 - Replaced DVI EMI caps with 0201 versions (p.22)
10/14/02 - Changed J18 to RJ45 with integrated magnetics (p.26)
10/15/02 - Moved Firewire connectors and port power switch to separate page (p.28)
Changed SMBus pullups to 2.15K, 1% as per iBooks/P84 [involved component net swaps] (p.29)
Added 0603 resistors as shorting pads for power up and reset (p.23)
Changed INT_MOD_SYNC, INT_MOD_DTI and INT_MOD_BITCLK to pulldowns per ERS [LA clk not used] (p.14)
Added damping resistor option to LMU crystal (p.23)
Changed INT_TST_PLLEN_PD to pulldown only [LA_clk not used] (p.13)
Changed JTAG_ENET_TDI to pullup [LA_clk not used] (p.13)
Removed FW_LKON from Intrepid EXTINT3 [no longer used], pullup added (p.14)
Changed BBANG_HRESET_L pullup to 3V_SLEEP (p.6)
Changed FW_PC_PD, FW_PC_PU resistors to 5% (p.27)
Added 1K pulldown and net FW_PD2 to FW_PHY (p.27)
10/16/02 - Implemented new FW power switch and current limit (p.28)
Renamed +14V_PBUS to +PBUS (p.all)
Added A29 adapter detection circuit (p.29)
Added +PBUS current limiting circuit, removed battery charging current limit circuit (p.30)
Changed FW_PHY_PIN_DS1 to pullup to make Port 1 1394A only (p.27)
10/21/02 - Updated CY28512 clock chip to Rev B (p.14)
Changed keyboard ZIF to large SMK connector (p.23)
Added full support for non-zero CPU_PLL_CFG<4> in run state (p.7)
10/22/02 - Mirrored wireless connector for P50 flex (p.24)
10/23/02 - Changed LMU/sleep LED interface per p84 (p.23)
Changed LMU JTAG/I2C pinout/pullup/pulldown strategy per P84 (p.23)
Changed fan FETs to Si3446DV per P84 (p.25)
Pinned out audio connector (p.25)
Pinned out right USB connector (p.25)
Pinned out modem connector (p.25)
Pinned out modem connector (p.25)
Added 2 functional test points to wireless connector (p.24,38)
Renamed FW low voltage power rails (p.27,37)
Renamed Vcore VID nets to be consistent with P84 (p.33)
Removed redundancy in DDR memory constraints (p.35)
10/24/02 - Changed FW_DS2 strap to pullup in stuff part 2 (p.27)
Cleaned up CY28512B circuit as per P84 (powered off main, output divider and strap tweaks] (p.14)
Updated PCI clock_series_R values per P84 (p.12)
Changed power rail for ALS to +3V_MAIN per P84 (p.23)
Added 0 ohm short and bypass cap for QVDDVO per P84 (p.21,37)
Split FW_VGND into FW_VGND0 and FW_VGND1 (p.28,37)
Added TP nets to GPU for XOR-tree testing (p.19-21)
Changed fan PWM output pullups to +3V_SLEEP to prevent pump-up (p.25)
10/28/02 - Added FW thermal pad ground hole back in (p.27)
Reopinned LMU pulldown for layout (p.23)
10/30/02 - Changed fan power rails to common Vet (p.25)
10/31/02 - Removed MLB ALS (p.23)
Added wireless RF_DISABLE_L pullup and AIRPORT_CLKRUN_L pulldown (p.24)
11/05/02 - Added 6 decoupling caps to CPU_VCORE_SLEEP (p.5)
Broke out quad OR-gate to discrete components for better placement (p.22,29)
11/06/02 - Changed 10 uF FW current limit output cap to two 4.7 uF caps (p.28)
Added 3 decoupling caps to CPU_VCORE_SLEEP (p.5)
Added 9 decoupling caps to each of +5V_MAIN and +3V_MAIN (p.32)
Removed XW17, jumper for CPU_VCORE_SLEEP (p.33)
Added decoupling cap to PMU reset OR gates (p.29)
11/08/02 - Changed firewire PHY to Z17 (p.27)
Added bulk caps to fan connectors (p.25)
Added alternate chassis gnd connection for sleep LED (p.23)
11/11/02 - Removed +3V_MAIN option for P50 card (p.24)
11/13/02 - Removed LMU and associated circuitry (p.23)
11/21/02 - Implemented D3cold for all PCI devices (p.12,14,18)
11/25/02 - Renamed all components (all pages)
11/26/02 - Removed chokes from 1394b data pairs (p.27,28)

EVT RELEASE

12/13/02 - Added 12 pF caps to source of 33MHz PCI clocks since they can not be buried (p.12)
Replaced ADM1031 with ADT7460 [I2C Address Change!] (p.25)
Added ADT7460 hookups to GPU thermal diode (p.21,25)
Added Firewire 8 ESD protection circuits (p.28)
12/16/02 - Removed hole from Firewire ground pad (p.27)
DDR memory connector renamed to J25 (p.11)
12/20/02 - Removed LT4210 from Firewire port power (p.28)
Added F10,F29 as placeholders and experiment guides (p.28)
Added diodes to OR +5V_SLEEP into FW_PHY power supply (p.27)
12/26/02 - Updated CPU p/ns to production p/ns (p.5)
Removed RC_glitch filter on CPU_DRDY_L (p.5,36)
Updated PCI source clock and internal spreading straps (p.8)
Changed BootROM PWD signal to INT_RESET_L per P84 (p.9)
Added CKE pulldowns per P84 (p.9)
Updated Ethernet series Rs per P84 [Clocks to 10 ohms, data to 22 ohms] (p.13)
Updated SSCG/NO_SSCG BOM options (p.14)
Renamed line-in and headphone sense lines to reflect active low signals (p.14,25.39)
Added 0 ohm Rs to make 2.5V_Intrepid rail hot or cold (p.15.16,38)
NO STUFFed RC filter + 1.5V LDO circuit (p.15)
Stuffed USB OC1/PPON signals for left/right ports (p.17,39)
Updated GPU VCore to stay in sync with P84 [after improvement] (p.20)
Added EMI caps to LVDS_DDC_CLK, INT_I2S0_SND_MCLK, INT_I2S0_SND_SCLK per P84 (p.22,25)
Added R800,R801 for eventual thermal diode in CPU (p.25)
Renamed R2009 to R799, R2001 to R802, R2002 to R803 (p.25)
Renamed F10 to F1, F20 to F2 [deleted old F1,F2] (p.28)
Added caps to FW ESD circuit that were missed (p.28)
Changed MAX4172 power source to save current on battery [per P84] (p.30)
Updated 1.5V/2.5V switcher BOM to stay in sync with P84 [FET change and current limits] (p.34)
Replaced all 1325i061 [1uF,0805,10V,20%] with 1325P046 [1uF,0603,10V,20%] (p.14,15,27,30,33,34)
Replaced all 1385B351 [1uF,0603,6.3V,10%] with 1325P046 [1uF,0603,10V,20%] (p.27,30)
01/02/03 - Updated FireWire fuse topology to that of P84 (p.28)
Updated system and power block diagrams (p.2,3)
01/03/03 - Corrected +2.5V_INTREPID connections to muxes and reference (p.9,10)
01/07/03 - Added NO_TEST nets to pads of DDR connector arms (p.11)
01/08/03 - Added 2N7002 circuits to ensure speakers are muted during power-up (p.25)
Changed R164 to 511 ohms to avoid low CPU clock amplitude (p.8)
01/09/03 - Added required pulldown to output of DVI HPD sense comparator (p.22)
Swapped R443 and R444 values to ensure Vgs < -4.5V (p.28)
Updated S-video filter values to those of P84 (p.22)
01/10/03 - ZT7,ZT23,ZT61,ZT76,ZT89,ZT87,ZT22,ZT38,ZT60,ZT42 & ZT17 are changed to HOLE-VIA-20R10 (p.4)
01/13/03 - Add L53, L54, L55 for TMDS Data<0:2> Diff Pair (p.22)
01/14/03 - Add C812 - C821 (Total 10 0.22uF caps) for 2.5V Intrepid Decoupling (p.16)
Add C822 & C823 at Wireless Card connector MAIN_RESET_L & RF_DISABLE_L_SPN (p.24)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Change MATCHED_DELAY to 50 for all TMDS DIFF PAIR (p.37)
Add R810 & R811 for ALWAYS-ON FANs in Acrylic Build (p.25)
01/28/03 - Remove NV31/17 components (p.19-21)
Add M10 (p.19-21)
02/07/03 - Add Power Net Constraints for M10 (p.38)
Replace Singing PBus Cap C49,C50,C67,C68,C80,C81,C95,C96,C108,C109,C120,C121 with 12630035 (for alt. 12650036) (p.33)
02/11/03 - Add FW Power Net Constraints (p.36)
Change signal constraints for AGP signals (p.36)
Add LMU connector and components (p.23)
Edit I2C table for LMU (p.13)
Change R500 to 19.6K (p.14)
Connect Clock Slewing RESET# to MAIN_RESET_L (p.14)
Change Ferrite Bean of ATI power supply to correct values (p.21)
Remove C141 PBUS CAP (p.31)
02/12/03 - Change and Rotate Keyboard Connector (p.23)
Add ATI Power sequencing Circuit for M10 Power-up and Power-down (p.19-22, p.32-35)

EVT RELEASE (continue)

02/13/03 - Add C825 (p.30)
02/17/03 - Rename all Reference Designators

EVT ENCLOSURE RELEASE

03/13/03 - Change 3-P FAN connectors to 4-P (p.25)
Add PU at PMU_SLEEP_LED_L for LMU (p.23)
Change stuffing option for clock slewing & PLL5 (p.14)
Change ATI M10 GPIO8 to Pull-down (p.20)
Remove Memory MUX 0ohm Resistors (p.10)
03/28/03 - Due to MLB outline change at DVI connector, CHGND1 has to be splitted into CHGND1 & CHGND2 (P 4 & 22)
Separate +3V and +5V traces running from 3/5V supply to 40Pin LIO connector (P 25 & 32)
R681 change from 100K to 4.7K (P 29)
Change airline detect to 13.1V or greater, R40 and R690 to 97.6K ohm (P 30 & 31)
Add C826 at U3 RS- pin (P 30)
Change D3 to 1N914 PN Junction Diode(P 31)
03/31/03 - Change AGPTEST Pull-up to 47ohm (it was 40ohm) (P 20)
Add circuits to prevent start-up Headphone POP (P 25)
Change all 1210 4.7uF to 1206 4.7uF Cap (1385P0531) (various pages)
Modify FAN circuit to PWM active low signal (P25)
04/08/03 - Add SOFT_MODEM_support (P 14 & 25)
Add 10-Pin ELCO connector for Serial Debug Interface (P 25)
Change Q7 from Si4435DY to SUD45P03-10 (P 30)
Remove D34 RS3AB (P 30)
04/11/03 - Change FW Schottky Diode to a 3A part 371S0159 (P 28)
Change PBUS L69 and VCORE L71 Inductor (P 31 & 33)
Change C643 10uF Cap to 1206 package part (P 28)
Change all 6 VCORE Caps to 220uF Al Poly Cap 128S0024 (P 33)
Add Mitsumi MM1571J regulator to provide 1.8V TPVDD (P 21)
Change U34 to Mitsumi MM1571J part for ATI PLL 1.8V rail(P 21)
04/16/03 - Add FW Port ShutDown/PowerOn Circuit (P 28)
Change the I2C Pull-up for Sound/Modem to 1K ohm (P 14)
04/17/03 - Change 3V/5V inductors (152S0137) L61 & L62 (P 32)
04/21/03 - Add 12 ICT JTAG TEST PADs (P 39)
04/23/03 - Invert ATI GPIO15 signal, no stuff pull-up resistor (P 20)
Combine Q35 and Q36 into a Dual Package Part (P 22)
SWAP the ADT7460 Temperature Sense pair (P 25)
Change FW PHY to production part (P 26)
04/24/03 - Remove +3V_CBUS_SLEEP and U5, use +3V_SLEEP directly (P 14,18,24)
Add 0402 Res between ATI PVDD/TPVDD rail and 10uF caps for stability purpose (P 21)
Add 90ohm common mode choke at TMDS data <0..2> pairs (P 22)
Add Sense Resistor to Vcore power rail, remove one 220uF cap <back to EVTA design> (P 33)
04/25/03 - Change C826 to 0.01uF 50V Cap (P 30)
04/30/03 - No stuff R676 to prevent +3V rail leakage (P 33)
05/02/03 - L45,L46,L47 is using Common Mode Choke TDK ACM2012D Part, will replace with ACM2012H Part if available (P 22)

DVT RELEASE

05/21/03 - Swap +PBUS and +24V_PBUS at Backup Battery Connector - J16 (P.31)
05/27/03 - Change R931 to 4.7K for I2c timing specification (P.13)
Change Q62 & Q65 to SI7336BDP part (P.33)
Change Q60, Q63 & Q66 to IRF7832 part and split C102 into 3 10pF caps (P.33)
Enable Vcore Burst(Skip) Mode by no stuffing R67 (P.33)
Enable 3V/5V Burst Mode by changing R406 & R407 to 100K ohm (P.32)
Change Q48 to SI7060DP part (P.20)
Change Q49 to IRF7832 part (P.20)
Enable GPUcore Burst Mode by changing R358 to 2.2 ohm, no stuffing R344 and stuffing R343 (P.20)
Reduce audible noise by changing L64 to 152S0139 (P.20)
Add C838, C840, C839, C844 & C845 10pF caps near the power switchers FETs (P.20, 32 & 34)
Change PWM_L_Fan input (both L&R_Fans) to +5V_SLEEP pull-up (P.25)
05/30/03 - Connect SLEEP_LED_DGND to digital ground instead of CHGNDS (P.23)
06/03/03 - Add CPU Core Voltage offset option circuit (P.33)
GPU Vcore on/off timing (P.20)
06/05/03 - Change FW-B connector to 514S0058 with internal shield pins (P.28)
06/06/03 - Add four 0ohm jumper, in case there is no sw support for the multi-stage VCore (P.38)
Change the +2.5V_Sleep FET to reduce Voltage drop on the rail (P.34)
06/12/03 - Change CBUS & USB2 REQ LINE Pullup to +3V_MAIN (P.12)
Add 0 ohm at USB AVSS_GND (P.17)
Change TMDS common mode choke to TDK ACM2012-900H part (P.22)
Change HD_DMACK_L pullup R213 to 10K (P.24)
Add C847, C851 & C852 at ENET CLK for EMC (P.13 & 26)
Change Q34 to FDS3672 (P.28)
Change Q82 pin#4 connection to system digital GND (P.33)
Add C848 150uF cap at J3 for +5V_MAIN USB2 power (P.25)
Add C853 1000pF cap at Q64 (P.30)
Add RC at ADT7460 power rail for noise isolation (P.25)
Isolate THERM# signal at ADT7460 by using double inverters for THERM_L_OC (P.25)
Remove redundant pullup R681 for THERM_L_OC (P.29)
Remove SH2 EMI spring at CHGND5 (P.23)
Add additional PWR/GND pins at J17 for R-USB board (P.25)
06/13/03 - New SODIMM connector with 4 through-hole mounting pins (P.11)
Change CPU config stuffing option at R83 and R64 (P.7)
Stuff R288 for Cypress CIR chip (P.14)
Move CBUS_PCI_REQ_L back to +3V_SLEEP rail pull-up (P.12)
Change the TMDS Termination Resistor values to 162ohm (P.20)
Connect C847 at R160_1 (P.13)
Add 1000pF caps at ADT7460 D_plus/minus pairs (P.25)
Add Si152 DVI transmitter to prevent leakage from DVI connector to the system (P.19&20)
06/16/03 - Replace C705,C707,C711,C703 & C685 with part 128S0025 (P.20&32)
Remove R271 0ohm resistor (P.32)
Edit Signal Constraints for TMDS routing and ENET routing (P.36&37)

DVT2 RELEASE

07/06/03 - Change R97 & R98 to 0402 package (P.33)
No Stuff R835 (P.19)
Change R198 to 100K ohm resistor (P.23)
Add Common Mode Choke L77 & L76 at FWB pairs (P.28)
Removed current monitoring IC for firewire port power (P.28)
Changed RP52,RP53,RP56,RP57 to 22ohm for EMI (P.19)

PRODUCTION RELEASE

07/28/03 - Change BOM option for C51,C52,C77,C78,C91,C92,C111 to 8.2uF Panasonic AL cap only (p. 34)
08/05/03 - Change +3V/5V ITH compensation and No-Stuff Feed Forward Caps (p. 32)
Change CPU VCORE setting for both BEST and BETTER configurations (p. 33)
08/07/03 - Change CPU VCORE setting for both BEST and BETTER configurations again (p. 33)

PRODUCTION RELEASE(Version C)

08/18/03 - Change CPU VCORE setting for BEST configuration to: 1.335V(High)->1.080V(Low) (p. 33)

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6338 | REV. C

SCALE NONE | SHT 40 OF 40

www.vinafix.vn